

Document Title***Multi-Chip Package MEMORY******64M Bit (4Mx16) Four Bank NOR Flash Memory / 16M Bit (1Mx16) Full CMOS SRAM*****Revision History**

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial Draft	August 29, 2001	Advance
1.0	Revised - Changed F-Vcc Max. Value (from 3.0V to 3.3V) - Added Endurance(100K Cycles)	November 27, 2001	Final

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Multi-Chip Package MEMORY

64M Bit (4Mx16) Four Bank NOR Flash Memory / 16M Bit (1Mx16) Full CMOS SRAM

FEATURES

- Power Supply voltage : 2.7 to 3.3 V
- Organization
 - Flash : 4,194,304 x 16 bit
 - SRAM : 1,048,576 x 16 bit
- Access Time (@2.7V)
 - Flash : 85 ns, SRAM : 55 ns
- Power Consumption (typical value)
 - Flash Read Current : 20 mA (@5MHz)
 - Sequential Page Read Current : 5 mA (@5MHz)
 - Program/Erase Current : 35 mA (Max.)
 - Standby mode/Deep Power mode : 0.1 μ A
 - SRAM Operating Current : 30 mA
 - Standby Current : 0.5 μ A
- Secode(Security Code) Block : Extra 32KW Block (Flash)
- Block Group Protection / Unprotection (Flash)
- 128 words Page Program (Flash)
- Flash Bank Size : 4Mb / 4Mb / 28Mb / 28Mb
- Flash Endurance : 100,000 Program/Erase Cycles
- SRAM Data Retention : 1.5 V (min.)
- Ambient Temperature : -40°C ~ 85°C
- Endurance : 100,000 Program/Erase Cycles
- Package : 81 - ball TBGA Type - 10.8 x 10.4 mm, 0.8 mm pitch

GENERAL DESCRIPTION

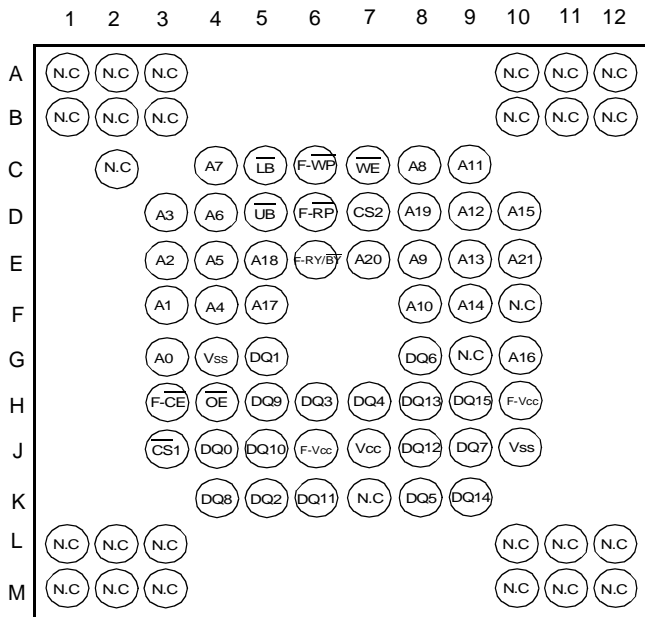
The K5C6417YT(B)M featuring single 3.0V power supply is a Multi Chip Package Memory which combines 64Mbit Four Bank Flash and 16Mbit CMOS SRAM.

The 64Mbit Flash memory is organized as 4M x16 bit and 16Mbit SRAM is organized as 1M x16 bit. The 64Mbit Flash memory is the high performance non-volatile memory fabricated by CMOS technology for peripheral circuit and DINOR IV(Divided bit-line NOR IV) architecture for the memory cell. All memory blocks are locked and can be programmed or erased, when F-WP is low. Using Software Lock Release function, program erase operation can be executed.

The 16Mbit SRAM supports low data retention voltage for battery backup operation with low data retention current.

The K5C6417YT(B)M is suitable for use in program and data memory of mobile communication system to reduce mount area. This device is available in 81-ball TBGA Type package.

BALL CONFIGURATION



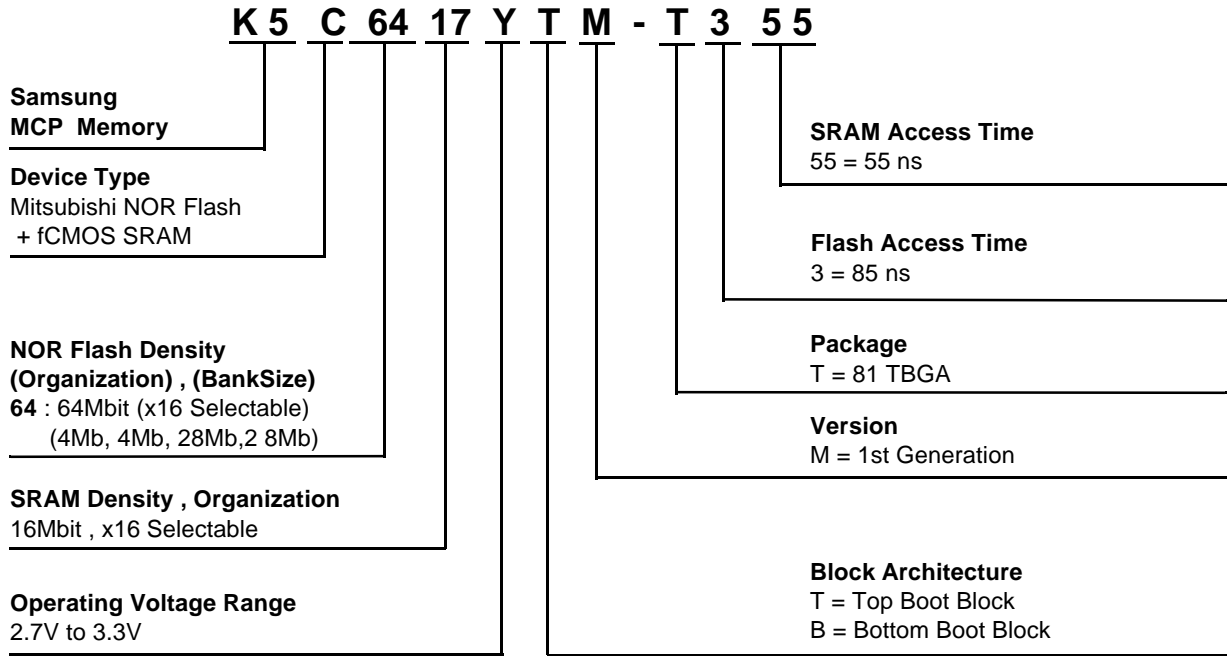
81 Ball TBGA , 0.8mm Pitch
Top View (Ball Down)

BALL DESCRIPTION

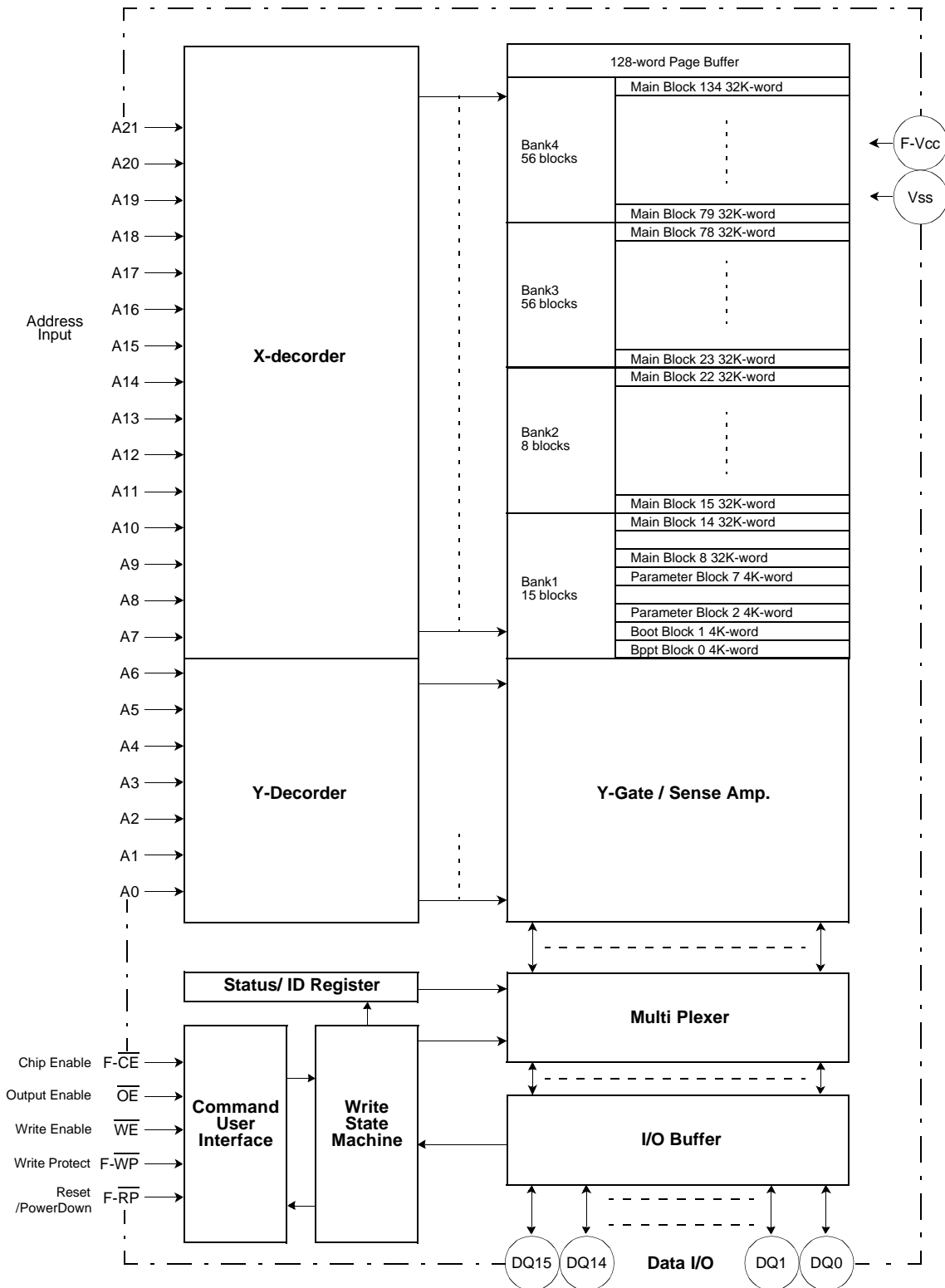
Ball Name	Description
A0 to A19	Address Input Balls (Common)
A20 to A21	Address Input Balls (Flash Memory)
DQ0 to DQ15	Data Input/Output Balls (Common)
F-RP	Hardware Reset (Flash Memory)
F-WP	Write Protect (Flash Memory)
F-Vcc	Power Supply (Flash Memory)
Vcc	Power Supply (SRAM)
Vss	Ground (Common)
UB	Upper Byte Enable (SRAM)
LB	Lower Byte Enable (SRAM)
F-CE	Chip Enable (Flash Memory)
CS1	Chip Enable (SRAM Low Active)
CS2	Chip Enable (SRAM High Active)
WE	Write Enable (Common)
OE	Output Enable (Common)
F-RY/BY	Ready/Busy (Flash memory)
N.C	No Connection

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ORDERING INFORMATION



Flash Memory Part



FUNCTIONAL BLOCK DIAGRAM (64Mbit Flash Memory)

Table 1. Flash Memory Top Boot Block Address (K5C6417YT)

K5C6417YT	Block	Block Size	Address Range
			Word Mode (x16)
Bank4	BA134	4 Kwords	3FF000H-3FFFFFFH
	BA133	4 Kwords	3FE000H-3FEFFFFH
	BA132	4 Kwords	3FD000H-3FDFFFFH
	BA131	4 Kwords	3FC000H-3FCFFFFH
	BA130	4 Kwords	3FB000H-3FBFFFFH
	BA129	4 Kwords	3FA000H-3FAFFFFH
	BA128	4 Kwords	3F9000H-3F9FFFFH
	BA127	4 Kwords	3F8000H-3F8FFFFH
	BA126	32 Kwords	3F0000H-3F7FFFFH
	BA125	32 Kwords	3E8000H-3EFFFFH
	BA124	32 Kwords	3E0000H-3E7FFFFH
	BA123	32 Kwords	3D8000H-3DFFFFH
	BA122	32 Kwords	3D0000H-3D7FFFFH
	BA121	32 Kwords	3C8000H-3CFFFFH
Bank3	BA119	32 Kwords	3B8000H-3BFFFFH
	BA118	32 Kwords	3B0000H-3B7FFFFH
	BA117	32 Kwords	3A8000H-3AFFFFH
	BA116	32 Kwords	3A0000H-3A7FFFFH
	BA115	32 Kwords	398000H-39FFFFH
	BA114	32 Kwords	390000H-397FFFFH
	BA113	32 Kwords	388000H-38FFFFH
	BA112	32 Kwords	380000H-387FFFFH
Bank2	BA111	32 Kwords	378000H-37FFFFH
	BA110	32 Kwords	370000H-377FFFFH
	BA109	32 Kwords	368000H-36FFFFH
	BA108	32 Kwords	360000H-367FFFFH
	BA107	32 Kwords	358000H-35FFFFH
	BA106	32 Kwords	350000H-357FFFFH
	BA105	32 Kwords	348000H-34FFFFH
	BA104	32 Kwords	340000H-347FFFFH
	BA103	32 Kwords	338000H-33FFFFH
	BA102	32 Kwords	330000H-337FFFFH
	BA101	32 Kwords	328000H-32FFFFH
	BA100	32 Kwords	320000H-327FFFFH
	BA99	32 Kwords	318000H-31FFFFH
	BA98	32 Kwords	310000H-317FFFFH
	BA97	32 Kwords	208000H-20FFFFH
	BA96	32 Kwords	300000H-307FFFFH
	BA95	32 Kwords	2F8000H-2FFFFFH
	BA94	32 Kwords	2F0000H-2F7FFFFH
BA93	32 Kwords	2E8000H-2EFFFFH	
BA92	32 Kwords	2E0000H-2E7FFFFH	
BA91	32 Kwords	2D8000H-2DFFFFH	
BA90	32 Kwords	2D0000H-2D7FFFFH	

Table 1. Flash Memory Top Boot Block Address (K5C6417YT)

K5C641TYT	Block	Block Size	Address Range
			Word Mode (x16)
Bank2	BA89	32 Kwords	2C8000H-2CFFFFH
	BA88	32 Kwords	2C0000H-2C7FFFH
	BA87	32 Kwords	2B8000H-2BFFFFH
	BA86	32 Kwords	2B0000H-2B7FFFH
	BA85	32 Kwords	2A8000H-2AFFFFH
	BA84	32 Kwords	2A0000H-2A7FFFH
	BA83	32 Kwords	298000H-29FFFFH
	BA82	32 Kwords	290000H-297FFFH
	BA81	32 Kwords	288000H-28FFFFH
	BA80	32 Kwords	280000H-287FFFH
	BA79	32 Kwords	278000H-27FFFFH
	BA78	32 Kwords	270000H-277FFFH
	BA77	32 Kwords	268000H-26FFFFH
	BA76	32 Kwords	260000H-267FFFH
	BA75	32 Kwords	258000H-25FFFFH
	BA74	32 Kwords	250000H-257FFFH
	BA73	32 Kwords	248000H-24FFFFH
	BA72	32 Kwords	240000H-247FFFH
	BA71	32 Kwords	238000H-23FFFFH
	BA70	32 Kwords	230000H-237FFFH
	BA69	32 Kwords	228000H-22FFFFH
	BA68	32 Kwords	220000H-227FFFH
	BA67	32 Kwords	218000H-21FFFFH
	BA66	32 Kwords	210000H-217FFFH
	BA65	32 Kwords	208000H-20FFFFH
	BA64	32 Kwords	200000H-207FFFH
	BA63	32 Kwords	1F8000H-1FFFFFH
	BA62	32 Kwords	1F0000H-1F7FFFH
	BA61	32 Kwords	1E8000H-1EFFFFH
	BA60	32 Kwords	1E0000H-1E7FFFH
	BA59	32 Kwords	1D8000H-1DFFFFH
	BA58	32 Kwords	1D0000H-1D7FFFH
BA57	32 Kwords	1C8000H-1CFFFFH	
BA56	32 Kwords	1C0000H-1C7FFFH	
Bank1	BA55	32 Kwords	1B8000H-1BFFFFH
	BA54	32 Kwords	1B0000H-1B7FFFH
	BA53	32 Kwords	1A8000H-1AFFFFH
	BA52	32 Kwords	1A0000H-1A7FFFH
	BA51	32 Kwords	198000H-19FFFFH
	BA50	32 Kwords	190000H-197FFFH
	BA49	32 Kwords	188000H-18FFFFH
	BA48	32 Kwords	180000H-187FFFH
	BA47	32 Kwords	178000H-17FFFFH
	BA46	32 Kwords	170000H-177FFFH
BA45	32 Kwords	168000H-16FFFFH	

Table 1. Flash Memory Top Boot Block Address (K5C6417YT)

K5C6417YT	Block	Block Size	Address Range
			Word Mode (x16)
Bank1	BA44	32 Kwords	16000H-167FFFH
	BA43	32 Kwords	158000H-15FFFFH
	BA42	32 Kwords	150000H-157FFFH
	BA41	32 Kwords	148000H-14FFFFH
	BA40	32 Kwords	140000H-147FFFH
	BA39	32 Kwords	138000H-13FFFFH
	BA38	32 Kwords	130000H-137FFFH
	BA37	32 Kwords	128000H-12FFFFH
	BA36	32 Kwords	120000H-127FFFH
	BA35	32 Kwords	118000H-11FFFFH
	BA34	32 Kwords	110000H-117FFFH
	BA33	32 Kwords	108000H-10FFFFH
	BA32	32 Kwords	100000H-107FFFH
	BA31	32 Kwords	F8000H-FFFFFH
	BA30	32 Kwords	F0000H-F7FFFH
	BA29	32 Kwords	E8000H-EFFFFH
	BA28	32 Kwords	E0000H-E7FFFH
	BA27	32 Kwords	D8000H-DFFFFH
	BA26	32 Kwords	D0000H-D7FFFH
	BA25	32 Kwords	C8000H-CFFFFH
	BA24	32 Kwords	C0000H-C7FFFH
	BA23	32 Kwords	B8000H-BFFFFH
	BA22	32 Kwords	B0000H-B7FFFH
	BA21	32 Kwords	A8000H-AFFFFH
	BA20	32 Kwords	A0000H-A7FFFH
	BA19	32 Kwords	98000H-9FFFFH
	BA18	32 Kwords	90000H-97FFFH
	BA17	32 Kwords	88000H-8FFFFH
	BA16	32 Kwords	80000H-87FFFH
	BA15	32 Kwords	78000H-7FFFFH
	BA14	32 Kwords	70000H-77FFFH
	BA13	32 Kwords	68000H-6FFFFH
BA12	32 Kwords	60000H-67FFFH	
BA11	32 Kwords	58000H-5FFFFH	
BA10	32 Kwords	50000H-57FFFH	
BA9	32 Kwords	48000H-4FFFFH	
BA8	32 Kwords	40000H-47FFFH	
BA7	32 Kwords	38000H-3FFFFH	
BA6	32 Kwords	30000H-37FFFH	
BA5	32 Kwords	28000H-2FFFFH	
BA4	32 Kwords	20000H-27FFFH	
BA3	32 Kwords	18000H-1FFFFH	
BA2	32 Kwords	10000H-17FFFH	
BA1	32 Kwords	08000H-0FFFFH	
BA0	32 Kwords	00000H-07FFFH	

Table 2. Flash Memory Bottom Boot Block Address (K5C6417YB)

K5C6417YB	Block	Block Size	Address Range
			Word Mode (x16)
Bank4	BA134	32 Kwords	3F8000H-3FFFFFFH
	BA133	32 Kwords	3F0000H-3F7FFFH
	BA132	32 Kwords	3E8000H-3EFFFFH
	BA131	32 Kwords	3E0000H-3E7FFFH
	BA130	32 Kwords	3D8000H-3DFFFFH
	BA129	32 Kwords	3D0000H-3D7FFFH
	BA128	32 Kwords	3C8000H-3CFFFFH
	BA127	32 Kwords	3C0000H-3C7FFFH
	BA126	32 Kwords	3B8000H-3BFFFFH
	BA125	32 Kwords	3B0000H-3B7FFFH
	BA124	32 Kwords	3A8000H-3AFFFFH
	BA123	32 Kwords	3A0000H-3A7FFFH
	BA122	32 Kwords	398000H-39FFFFH
	BA121	32 Kwords	390000H-397FFFH
	BA120	32 Kwords	388000H-38FFFFH
	BA119	32 Kwords	380000H-387FFFH
	BA118	32 Kwords	378000H-37FFFFH
	BA117	32 Kwords	370000H-377FFFH
	BA116	32 Kwords	368000H-36FFFFH
	BA115	32 Kwords	360000H-367FFFH
	BA114	32 Kwords	358000H-35FFFFH
	BA113	32 Kwords	350000H-357FFFH
	BA112	32 Kwords	348000H-34FFFFH
	BA111	32 Kwords	340000H-347FFFH
	BA110	32 Kwords	338000H-33FFFFH
	BA109	32 Kwords	330000H-337FFFH
	BA108	32 Kwords	328000H-32FFFFH
	BA107	32 Kwords	320000H-327FFFH
	BA106	32 Kwords	318000H-31FFFFH
	BA105	32 Kwords	310000H-317FFFH
	BA104	32 Kwords	208000H-20FFFFH
	BA103	32 Kwords	300000H-307FFFH
BA102	32 Kwords	2F8000H-2FFFFFFH	
BA101	32 Kwords	2F0000H-2F7FFFH	
BA100	32 Kwords	2E8000H-2EFFFFH	
BA99	32 Kwords	2E0000H-2E7FFFH	
BA98	32 Kwords	2D8000H-2DFFFFH	
BA97	32 Kwords	2D0000H-2D7FFFH	
BA96	32 Kwords	2C8000H-2CFFFFH	
BA95	32 Kwords	2C0000H-2C7FFFH	
BA94	32 Kwords	2B8000H-2BFFFFH	
BA93	32 Kwords	2B0000H-2B7FFFH	
BA92	32 Kwords	2A8000H-2AFFFFH	
BA91	32 Kwords	2A0000H-2A7FFFH	
BA90	32 Kwords	298000H-29FFFFH	

Table 2. Flash Memory Bottom Boot Block Address (K5C6417YB)

K5C6417YB	Block	Block Size	Address Range
			Word Mode (x16)
Bank4	BA89	32 Kwords	290000H-297FFFH
	BA88	32 Kwords	288000H-28FFFFH
	BA87	32 Kwords	280000H-287FFFH
	BA86	32 Kwords	278000H-27FFFFH
	BA85	32 Kwords	270000H-277FFFH
	BA84	32 Kwords	268000H-26FFFFH
	BA83	32 Kwords	260000H-267FFFH
	BA82	32 Kwords	258000H-25FFFFH
	BA81	32 Kwords	250000H-257FFFH
	BA80	32 Kwords	248000H-24FFFFH
Bank3	BA79	32 Kwords	240000H-247FFFH
	BA78	32 Kwords	238000H-23FFFFH
	BA77	32 Kwords	230000H-237FFFH
	BA76	32 Kwords	228000H-22FFFFH
	BA75	32 Kwords	220000H-227FFFH
	BA74	32 Kwords	218000H-21FFFFH
	BA73	32 Kwords	210000H-217FFFH
	BA72	32 Kwords	208000H-20FFFFH
	BA71	32 Kwords	200000H-207FFFH
	BA70	32 Kwords	1F8000H-1FFFFFH
	BA69	32 Kwords	1F0000H-1F7FFFH
	BA68	32 Kwords	1E8000H-1EFFFFH
	BA67	32 Kwords	1E0000H-1E7FFFH
	BA66	32 Kwords	1D8000H-1DFFFFH
	BA65	32 Kwords	1D0000H-1D7FFFH
	BA64	32 Kwords	1C8000H-1CFFFFH
	BA63	32 Kwords	1C0000H-1C7FFFH
	BA62	32 Kwords	1B8000H-1BFFFFH
	BA61	32 Kwords	1B0000H-1B7FFFH
	BA60	32 Kwords	1A8000H-1AFFFFH
	BA59	32 Kwords	1A0000H-1A7FFFH
	BA58	32 Kwords	198000H-19FFFFH
	BA57	32 Kwords	190000H-197FFFH
	BA56	32 Kwords	188000H-18FFFFH
	BA55	32 Kwords	180000H-187FFFH
	BA54	32 Kwords	178000H-17FFFFH
	BA53	32 Kwords	170000H-177FFFH
	BA52	32 Kwords	168000H-16FFFFH
	BA51	32 Kwords	160000H-167FFFH
	BA50	32 Kwords	158000H-15FFFFH
	BA49	32 Kwords	150000H-157FFFH
	BA48	32 Kwords	148000H-14FFFFH
	BA47	32 Kwords	140000H-147FFFH
	BA46	32 Kwords	138000H-13FFFFH
BA45	32 Kwords	130000H-137FFFH	

Table 2. Flash Memory Bottom Boot Block Address (K5C6417YB)

K5C6417YB	Block	Block Size	Address Range	
			Word Mode (x16)	
Bank3	BA44	32 Kwords	128000H-12FFFFH	
	BA43	32 Kwords	120000H-127FFFH	
	BA42	32 Kwords	118000H-11FFFFH	
	BA41	32 Kwords	110000H-117FFFH	
	BA40	32 Kwords	108000H-10FFFFH	
	BA39	32 Kwords	100000H-107FFFH	
	BA38	32 Kwords	F8000H-FFFFFH	
	BA37	32 Kwords	F0000H-F7FFFH	
	BA36	32 Kwords	E8000H-EFFFFH	
	BA35	32 Kwords	E0000H-E7FFFH	
	BA34	32 Kwords	D8000H-DFFFFH	
	BA33	32 Kwords	D0000H-D7FFFH	
	BA32	32 Kwords	C8000H-CFFFFH	
	BA31	32 Kwords	C0000H-C7FFFH	
	BA30	32 Kwords	B8000H-BFFFFH	
	BA29	32 Kwords	B0000H-B7FFFH	
	BA28	32 Kwords	A8000H-AFFFFH	
	BA27	32 Kwords	A0000H-A7FFFH	
	Bank2	BA26	32 Kwords	98000H-9FFFFH
		BA25	32 Kwords	90000H-97FFFH
BA24		32 Kwords	88000H-8FFFFH	
BA23		32 Kwords	80000H-87FFFH	
BA22		32 Kwords	78000H-7FFFFH	
BA21		32 Kwords	70000H-77FFFH	
BA20		32 Kwords	68000H-6FFFFH	
BA19		32 Kwords	60000H-67FFFH	
Bank1	BA18	32 Kwords	58000H-5FFFFH	
	BA17	32 Kwords	50000H-57FFFH	
	BA16	32 Kwords	48000H-4FFFFH	
	BA15	32 Kwords	40000H-47FFFH	
	BA14	32 Kwords	38000H-3FFFFH	
	BA13	32 Kwords	30000H-37FFFH	
	BA12	32 Kwords	28000H-2FFFFH	
	BA11	32 Kwords	20000H-27FFFH	
	BA10	32 Kwords	18000H-1FFFFH	
	BA9	32 Kwords	10000H-17FFFH	
	BA8	32 Kwords	08000H-0FFFFH	
	BA7	4 Kwords	07000H-07FFFH	
BA6	4 Kwords	06000H-06FFFH		
BA5	4 Kwords	05000H-05FFFH		
BA4	4 Kwords	04000H-04FFFH		
BA3	4 Kwords	03000H-03FFFH		
BA2	4 Kwords	02000H-02FFFH		
BA1	4 Kwords	01000H-01FFFH		
BA0	4 Kwords	00000H-00FFFH		

Flash MEMORY COMMAND DEFINITION

Table 3. Command List (F-WP = VIH or VIL)

Command	1st Cycle			2nd Cycle			3rd Cycle			
	Mode	Address	Data ¹⁾ (DQ0-15)	Mode	Address		Data ¹⁾ (DQ0-15)	Mode	Address	Data ¹⁾ (DQ0-15)
					A21-A18	A0				
Read Array	Write	X	FFH							
Sequential Page Read	Write	X	F3H	Read	SA ⁵⁾		RD0	Read	SA+i ⁶⁾	RDi
Device Identifier	Write	Bank ²⁾	90H	Read	Bank ²⁾	IA ³⁾	ID			
Read Status Register	Write	Bank ²⁾	70H	Read	Bank ²⁾		SRD ⁴⁾			
Clear Status Register	Write	X	50H							
Suspend	Write	Bank ²⁾	B0H							
Resume	Write	Bank ²⁾	D0H							

- Notes :**
1. Upper byte data (DQ15-DQ8) is ignored.
 2. Bank=Bank address (bank1-Bank4:A21-18)
 3. IA=ID code address:A0=VIL (Manufacture's code):A0=VIH (Device code), ID=ID code
 4. SRD=Status Register Data
 5. SA=Sequential page Address:A21-A3, A2-A0:0h
 6. SA+i;A21-A3 must be fixed and A2-A0 must be incremented from 0h to 7h.

Table 4. Command List (F-WP = VIH)

Command	1st Cycle			2nd Cycle			3rd Cycle		
	Mode	Address	Data ¹⁾ (DQ0-15)	Mode	Address	Data ¹⁾ (DQ0-15)	Mode	Address	Data ¹⁾ (DQ0-15)
Word Program	Write	Bank	40H	Write	WA ²⁾	WD ²⁾			
Page Program	Write	Bank	41H	Write	WA0 ³⁾	WD0 ³⁾	Write	WAN ³⁾	WDn ³⁾
Page Buffer to Flash	Write	Bank	0EH	Write	WA ⁴⁾	D0 ¹⁾			
Block Erase / Confirm	Write	Bank	20H	Write	BA ⁵⁾	D0 ¹⁾			
Erase All Unlocked Blocks	Write	X	A7H	Write	X	D0 ¹⁾			
Clear Page Buffer	Write	X	55H	Write	X	D0 ¹⁾			
Single Date Load to Page Buffer	Write	Bank	74H	Write	WA	WD			
Flash to Page Buffer	Write	Bank	F1H	Write	RA ⁶⁾	D0 ¹⁾			

- Notes :**
1. Upper byte data (DQ15-DQ8) is ignored.
 2. WA=Write Address, WD=Write Data
 3. WA0, WAN=Write Address, WD0, WDn=Write Data, Write address and write data must be provided sequentially from 00H to 7FH for A6-A0. Page size is 128 words (128-word x 16-bit), and also A21-A7(block address, page address) must be valid.
 4. WA=Write Address:A21-A7 (block address, page address) must be valid.
 5. BA=Block Address:A21-A12(Bank1), A21-A15(Bank2, Bank3, Bank4)
 6. RA=Read Address:A21-A7 (block address, page address) must be valid.

Flash MEMORY COMMAND DEFINITION

Software lock release operation needs following consecutive 7bus cycles. Moreover, additional 127 bus cycles are needed for page program operation.

Table 5. Command List (F-WP = VIH or VIL)

Setup Command for Software Lock Release	1st Cycle			2nd Cycle			3rd Cycle		
	Mode	Address	Data ¹⁾ (DQ0-15)	Mode	Address	Data ¹⁾ (DQ0-15)	Mode	Address	Data ¹⁾ (DQ0-15)
Word Program	Write	Bank	60H	Write	Bank	Block ⁶⁾	Write	Bank	ACH
Page Program ³⁾	Write	Bank	60H	Write	Bank	Block ⁶⁾	Write	Bank	ACH
Page Buffer to Flash	Write	Bank	60H	Write	Bank	Block ⁶⁾	Write	Bank	ACH
Block Erase / Confirm	Write	Bank	60H	Write	Bank	Block ⁶⁾	Write	Bank	ACH
Erase All Unlocked Blocks	Write	Bank	60H	Write	Bank	Block ⁶⁾	Write	Bank	ACH
Clear Page Buffer	Write	Bank	60H	Write	Bank	Block ⁶⁾	Write	Bank	ACH
Single Data Load to Page Buffer	Write	Bank	60H	Write	Bank	Block ⁶⁾	Write	Bank	ACH
Flash to Page Buffer	Write	Bank	60H	Write	Bank	Block ⁶⁾	Write	Bank	ACH

Setup Command for Software Lock Release	4th Cycle			5th Cycle		
	Mode	Address	Data ¹⁾ (DQ0-15)	Mode	Address	Data ¹⁾ (DQ0-15)
Word Program	Write	Bank	Block ⁶⁾	Write	Bank	78H
Page Program ³⁾	Write	Bank	Block ⁶⁾	Write	Bank	78H
Page Buffer to Flash	Write	Bank	Block ⁶⁾	Write	Bank	78H
Block Erase / Confirm	Write	Bank	Block ⁶⁾	Write	Bank	78H
Erase All Unlocked Blocks	Write	Bank	Block ⁶⁾	Write	Bank	78H
Clear Page Buffer	Write	Bank	Block ⁶⁾	Write	Bank	78H
Single Data Load to Page Buffer	Write	Bank	Block ⁶⁾	Write	Bank	78H
Flash to Page Buffer	Write	Bank	Block ⁶⁾	Write	Bank	78H

Setup Command for Software Lock Release	6th Cycle			7th Cycle			8th-134th Cycle		
	Mode	Address	Data ¹⁾ (DQ0-15)	Mode	Address	Data ¹⁾ (DQ0-15)	Mode	Address	Data ¹⁾ (DQ0-15)
Word Program	Write	Bank	40h	Write	WA ²⁾	WD ²⁾			
Page Program ³⁾	Write	Bank	41h	Write	WA0 ³⁾	WD0 ³⁾	Write	WAn ³⁾	WDn ³⁾
Page Buffer to Flash	Write	Bank	0Eh	Write	WA ⁴⁾	D0 ¹⁾			
Block Erase / Confirm	Write	Bank	20H	Write	BA ⁵⁾	D0 ¹⁾			
Erase All Unlocked Blocks	Write	X	A7H	Write	X	D0 ¹⁾			
Clear Page Buffer	Write	X	55H	Write	X	D0 ¹⁾			
Single Data Load to Page Buffer	Write	Bank	74H	Write	WA	WD			
Flash to Page Buffer	Write	Bank	F1H	Write	RA ⁷⁾	D0 ¹⁾			

- Notes :**
- Upper byte data (DQ15-DQ8) is ignored.
 - WA=Write Address, WD=Write Data
 - WA0, WAn=Write Address, WD0, WDn=Write Data, Write address and write data must be provided sequentially from 00H to 7FH for A6-A0. Page size is 128 words (128 word x 16 bit), and also A21-A7(block address, page address) must be valid.
 - WA=Write Address:A21-A7 (block address, page address) must be valid.
 - BA=Block Address:A21-A12(Bank1), A21-A15(Bank2, Bank3, Bank4)
 - Block=Block Address:A21-A15, Block=A21-A15

Address	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Block	Fixed0	A21	A20	A19	A18	A17	A16	A15
Block	Fixed0	A21	A20	A19	A18	A17	A16	A15

- RA=Read Address: A21-A7 (block address, page address) must be valid.

Table 6. Device ID Code

Code \ Pins	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Hex Date
Manufacturer Code	V _{IL}	"0"	"0"	"0"	"1"	"1"	"1"	"0"	"0"	1CH
Devide Code (Bottom Boot)	V _{IH}	"0"	"0"	"1"	"0"	"1"	"0"	"1"	"0"	2AH
Devide Code (Top Boot)	V _{IH}	"0"	"0"	"1"	"0"	"1"	"0"	"1"	"1"	2BH

The output of upper byte data (DQ15-DQ7) is "0".

Table 7. Block Locking

F- $\overline{\text{RP}}$	F- $\overline{\text{WP}}$	Write Protection Provided					Notes
		Bank1		Bank2	Bank3	Bank4	
		Boot	Parameter/Main	Main	Main	Main	
V _{IL}	x	Locked	Locked	Locked	Locked	Locked	Deep Power Down Mode
V _{IH}	V _{IL}	Locked	Locked	Locked	Locked	Locked	All Blocks Locked (Valid to operate Software Lock Release)
	V _{IH}	Unlocked	Unlocked	Unlocked	Unlocked	Unlocked	All Blocks Unlocked

F- $\overline{\text{WP}}$ pin must not be switched during performing Read / Write operations or WSM busy (WSMS=0).

Table 8. Status Register

Symbol (I/O Pin)	Status	Definition	
		"1"	"0"
S.R.7 (AQ7)	Write State Machine Status	Ready	Busy
S.R.6 (DQ6)	Suspend Status	Suspended	Operation in Progress/Completed
S.R.5 (DQ5)	Erase Status	Error	Successful
S.R.4 (DQ4)	Program Status	Error	Successful
S.R.3 (DQ3)	Block Status after Program	Error	Successful
S.R.2 (DQ2)	Reserved	-	-
S.R.1 (DQ1)	Reserved	-	-
S.R.0 (DQ0)	Reserved	-	-

Table 9. Flash Memory Operation Table

Mode \ Pins		F- $\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	F- $\overline{\text{RP}}$	DQ0-15
Read	Array	V _{IL}	V _{IL}	V _{IH}	V _{IH}	Data-Output
	Sequential	V _{IL}	V _{IL}	V _{IH}	V _{IH}	Data-Output
	Status Register	V _{IL}	V _{IL}	V _{IH}	V _{IH}	Status Register Data
	Identifier Code	V _{IL}	V _{IL}	V _{IH}	V _{IH}	Identifier Code
Output Disable		V _{IL}	V _{IH}	V _{IH}	V _{IH}	High-Z
Write	Program	V _{IL}	V _{IH}	V _{IL}	V _{IH}	Command / Data-In
	Erase	V _{IL}	V _{IH}	V _{IL}	V _{IH}	Command
	Others	V _{IL}	V _{IH}	V _{IL}	V _{IH}	Command
Standby		V _{IH}	X ¹⁾	X	V _{IH}	High-Z
Deep Power Down		X	X	X	V _{IL}	High-z

Notes : 1. X cab be V_{IH} or V_{IL} for control pins

Flash DEVICE OPERATION

The 64Mbit DINOR IV Flash Memory includes on-chip program/erase control circuitry. The Write State Machine(WSM) control block erase and word/page program operations. Operational modes are selected by the commands written to the Command User Interface (CUI). The Status Register indicates the status of the WSM and when the WSM successfully completes the desired program or block erase operation.

A Deep Power Down mode is enabled when the $\overline{F-RP}$ pin is at Vss, minimizing power consumption.

Read Mode

The 64Mbit DINOR IV Flash Memory has four read modes, which accesses to the memory array, the Sequential Page Read, the Device Identifier and the Status Register. The appropriate read commands are required to be written to the CUI. Upon initial device power up or after exit from deep power down, the 64Mbit DINOR IV Flash Memory automatically resets to read array mode. In the read array mode and in the conditions are low level input to \overline{OE} , high level input to \overline{WE} and $\overline{F-RP}$, low level input to $\overline{F-CE}$ and address signals to the address inputs (A21 - A0) the data of the addressed location to the data input/output (DQ15-DQ0) is output.

Standby Mode

When $\overline{F-CE}$ is at V_{IH} , the device is in the standby mode and its power consumption is reduced. Data input/output are in a high-impedance (High-Z) state. If the memory is deselected during block erase or program, the internal control circuits remain active and the device consumes normal active power until the operation completes.

Output Disable

When \overline{OE} is at V_{IH} , output from the devices is disabled. Data input/output are in a high-impedance (High-Z) state.

Automatic Power Down (APD)

The Automatic Power Down minimizes the power consumption during read mode. The device automatically turns to this mode when any addresses or $\overline{F-CE}$ isn't changed more than 200ns after the last alternation. The power consumption becomes the same as the stand-by mode. During this mode, the output data is latched and can be read out. New data is read out correctly when addresses are changed.

Deep Power Down

When $\overline{F-RP}$ is at V_{IL} , the device is in the deep power down mode and its power consumption is substantially low. During read modes, the memory is deselected and the data input/output are in a high-impedance (High-Z) state. After return from power down, the CUI is reset to Read Array, and the Status Register is cleared to value 80H. During block erase or program modes, $\overline{F-RP}$ low will abort either operation. Memory array data of the block being altered become invalid.

Write Mode

Writes to the CUI enables reading of memory array data, device identifiers and reading and clearing of the Status Register. They also enable block erase and program. The CUI is written by bringing \overline{WE} to low level and \overline{OE} is at high level, while $\overline{F-CE}$ is at low level. Address and data are latched on the earlier rising edge of \overline{WE} and $\overline{F-CE}$. Standard micro processor write timings are used.

Alternating Background Operation (BGO)

The 64Mbit DINOR IV Flash Memory allows to read array from one bank while the other bank operates in software command write cycling or the erasing / programming operation in the background. Array Read operation with the other bank in BGO is performed by changing the bank address without any additional command. When the bank address points the bank in software command write cycling or the erasing / programming operation, the data is read out from the status register. The access time with BGO is the same as the normal read operation. BGO must be between Bank1, Bank2, Bank3, and Bank4.

Back Bank array Read (BBR)

In the 64Mbit DINOR IV Flash Memory, when one memory address is read according to a Read Mode in the case of the same as an access when a Read Mode command is input, another Bank memory data can be read out (Random or Sequential Mode) by changing another Bank address.

Software Command Definitions

The device operations are selected by writing specific software command into the Command User Interface.

Read Array Command (FFH)

The device is in Read Array mode on initial device power up and after exit from deep power down, or by writing FFH to the Command User Interface. After starting the internal operation the device is set to the read status register mode automatically.

Sequential Page Read Command (F3H)

The Sequential Page Read command (F3H) timing can be used by writing the first command. This command is fast sequential 8 words read. During the read it is necessary to fix $\overline{F-CE}$ low and increase the addresses sequentially from 0h to 7h. The mode is kept until Read Array command is input. The first read of Seq. Page Read timing is the same as normal read ($t_{a(CE)}$). $\overline{F-CE}$ should be fallen "L". The read timing after the first is fast read ($t_{a(PAD)}$). When an another sequential page (A21-A3) is accessed before one sequential page (one 8-word) read is not finished, once $\overline{F-CE}$ is at V_{IH} and A2-A0 data are 0h, after that $\overline{F-CE}$ is at V_{IL} we can use the first read of Seq. Page Read or normal read ($t_{a(CE)}$).

Read Device Identifier Command (90H)

We can normally read device identifier codes when Read Device Identifier Code Command (90H) is written to the command latch. Following the command write, the manufacturer code and the device code can be read from address 0000H and 0001H, respectively.

Read Status Register Command (70H)

The Status Register is read after writing the Read Status Register command of 70H to the Command User Interface. Also, after starting the internal operation the device is set to the Read Status Register mode automatically. The contents of Status Register are latched on the later falling edge of \overline{OE} must be toggled every status read.

Clear Status Register Command (50H)

The Erase Status, Program Status and Block Status bits are set to "1"s by the Write State Machine and can only be reset by the Clear Status Register command of 50H. These bits indicate various failure conditions. status read.

Block Erase / Confirm Command (20H/D0H)

Automated block erase is initiated by writing the Block Erase command of 20H followed by the Confirm command of D0H. An address within the block to be erased is required. The WSM executes iterative erase pulse application and erase verify operation.

Program Commands**1) Word Program (40H)**

Word program is executed by a two-command sequence. The Word program Setup command of 40H is written to the Command Interface, followed by a second write specifying the address and data to be written. The WSM controls the program pulse application and verify operation.

2) Page Program for Data Blocks (41H)

Page Program allows fast programming of 128words of data. Writing of 41H initiates the page program operation for the Data area. From 2nd cycle to 129th cycle, write data must be serially inputted. Address A6-A0 have to be incremented from 00H to 7FH. After completion of data loading, the WSM controls the program pulse application and verify operation.

3) Single Data Load to Page Buffer (74H) / Page Buffer to Flash (0EH/D0H)

Single data load to the page buffer is performed by writing 74H followed by a second write specifying the column address and data. Distinct data up to 128word can be loaded to the page buffer by this two-command sequence. On the other hand, all of the loaded data to the page buffer is programmed simultaneously by writing Page Buffer to Flash command of 0EH followed by the confirm command of D0H. After completion of programming the data on the page buffer is cleared automatically.

Flash to Page Buffer Command (F1H/D0H)

Array data load to the page buffer is performed by writing the Flash to Page Buffer command of F1H followed by the Confirm command of D0H. An address within the page to be loaded is required. Then the array data can be copied into the other pages within the same bank by using the Page Buffer to Flash command.

Clear Page Buffer Command (55H/D0H)

Loaded data to the page buffer is cleared by writing the Clear Page Buffer command of 55H followed by the Confirm command of D0H. This command is valid for clearing data loaded by Single Data Load to Page Buffer command.

Suspend/Resume Command (B0H/D0H)

Writing the Suspend command of B0H during block erase operation interrupts the block erase operation and allows read out from another block of memory. Writing the Suspend command of B0H during program operation interrupts the program operation and allows read out from another block of memory. The Bank address is required when writing the Suspend/Resume Command. The device continues to output Status Register data when read, after the Suspend command is written to it. Polling the WSM Status and Suspend Status bits will determine when the erase operation or program operation has been suspended. At this point, writing of the Read Array command to the CUI enables reading data from blocks other than that which is suspended. When the Resume command of D0H is written to the CUI, the WSM will continue with the erase or program processes.

Data Protection

The 64M-bit DINOR(IV) Flash Memory has a master Write Protect pin ($\overline{F-WP}$). When $\overline{F-WP}$ is at V_{IH} , all blocks can be programmed or erased. When $\overline{F-WP}$ is low, all blocks are in locked mode which prevents any modifications to memory blocks. Software Lock Release function is only command which allows to program or erase. See the BLOCK LOCKING table on 13 page for details.

Power Supply Voltage

When the power supply voltage is less than V_{LKO} , Low Vcc Lock-Out voltage, the device is set to the Read-only mode. Regarding DC electrical characteristics of V_{LKO} , see 18 page. A delay time of 2 μ s is required before any device operation is initiated. The delay time is measured from the time Vcc reaches V_{ccmin} (2.7V). During power up, $\overline{F-RP} = V_{SS}$ is recommended. Falling in Busy status is not recommended for possibility of damaging the device.

Memory Organization

The 64Mbit DINOR IV Flash Memory is constructed by 2 boot blocks of 4K words, 6 parameter blocks of 4K words and 7 main blocks of 32K words in Bank1, by 8 main blocks of 32K words in Bank2 and by 56 main blocks of 32K words in Bank3 and Bank4.

CAPACITANCE

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	TA=25°C, f=1MHz,		8	pF
Output Capacitance	C_{OUT}	Vin=Vout=0V		12	pF

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Unit
F-Vcc Voltage	F-Vcc	With Respect to Vss	-0.2 to +4.6	V
All input or Output Voltage ¹⁾	VI1		-0.6 to +4.6	
Ambient Temperature	Ta		-40 to +85	°C
Temperature under Bias	Tbs		-50 to +95	
Storage Temperature	Tstg		-65 to +125	
Outputs Short Circuit Current	Iout		100 (Max.)	mA

Notes : 1. Minimum DC voltage is -0.5V on input / output pins. During transitions, the level may undershoot to -2.0V for periods <20ns.
Maximum DC voltage on input / output pins is F-Vcc+0.5V which, during transitions, may overshoot to F-Vcc+1.5V for periods <20ns.

DC CHARACTERISTICS

Parameter	Sym- bol	Test Conditions	Min	Typ ¹⁾	Max	Unit
Input Leakage Current	ILI	$0V < V_{IN} < F-V_{CC}$			±1.0	μA
Output Leakage Current	ILO	$0V < V_{OUT} < F-V_{CC}$			±1.0	μA
Vcc Standby Current	ISB1	F-Vcc=3.3V, VIN=VIL/VIH, F-CE=F-RP=F-WP=VIH		50	200	μA
	ISB2	F-Vcc=3.3V, VIN=Vss/F-Vcc, F-CE=F-RP=F-WP=F-Vcc±0.3V		0.1	5	μA
Vcc Deep Power Down Current	ISB3	F-Vcc=3.3V, VIN/VIH, F-RP=VIL		5	15	μA
	ISB4	F-Vcc=3.3V, VIN=Vss or F-Vcc, F-RP=F-Vss±0.3V		0.1	5	μA
Vcc Read Current for Word	Icc1	F-Vcc=3.3V, VIN=VIL/VIH, F-RP=WE=VIH, F-CE=OE=VIL, Iout=0mA	5MHz	20	30	mA
Vcc Sequential Page Read Current	Icc1P	F-Vcc=3.3V, VIN=VIL/VIH, F-RP=WE=VIH, F-CE=OE=VIL, Iout=0mA	1MHz	4	8	mA
			5MHz	5	10	mA
Vcc Write Current for Word	Icc2	F-Vcc=3.3V, VIN=VIL/VIH, F-RP=OE=VIH, F-CE=WE=VIL			15	mA
Vcc Program Current	Icc3	F-Vcc=3.3V, VIN=VIL/VIH, F-CE=F-RP=F-WP=VIH			35	mA
Vcc Erase Current	Icc4	F-Vcc=3.3V, VIN=VIL/VIH, F-CE=F-RP=F-WP=VIH			35	mA
Vcc Suspend Current	Icc5	F-Vcc=3.3V, VIN=VIL/VIH, F-CE=F-RP=F-WP=VIH			200	mA
Input Low Voltage	VIL		-0.5		0.8	V
Input High Voltage	VIH		2.0		F-Vcc +0.5	V
Output Low Voltage	VOL	IOL=4.0mA			0.45	V
Output High Voltage	VOH1	Ioh=-2.0mA	0.85x F-Vcc			V
	VOH2	IOL=4-100μA	F-Vcc -0.4			V
Low F-Vcc Lock Out Voltage ²⁾	VLKO		1.5		2.2	V

Notes : All currents are in RMS unless otherwise noted

1. Typical values at F-Vcc=3.0V, Ta=25°C.

2. To protect initiation of write cycle during F-Vcc power up / down, a write cycle is locked out for F-Vcc less than VLKO, Write State Machine is in Busy state, if F-Vcc is less than VLKO, the alteration of memory contents may occur.

AC CHARACTERISTICS

Read Only Mode

Parameter	Symbol		Vcc=2.7V~3.3V			Unit
			Min	Typ	Max	
Read Cycle Time	tRC	tAVAV	85			ns
Address Access Time	ta(AD)	tAVQV			85	ns
Chip Enable Access Time	ta(CE)	tELQV			85	ns
Output Enable Access Time	ta(OE)	tGLQV			30	ns
Sequential Page Access Time (After 2nd Cycle)	ta(PAD)				45	ns
Sequential Page Setup Time	tASPR		-20			ns
Sequential Page Read F- $\overline{\text{CE}}$ "H" Time	tCEHRR		15			ns
Maximum Valid Time of Sequential Page Read	tRPCRR				20	ns
Chip Enable to Output in Low-Z	tCLZ	tELQX	0			ns
Chip Enable High to Output in High-Z	tDF(CE)	tEHQZ			25	ns
Output Enable to Output in Low-Z	tOLZ	tGLQX	0			ns
Output Enable to High to Output in High-Z	tDF(OE)	tGHQZ			25	ns
F- $\overline{\text{RP}}$ Low to Output High-Z	tPHZ	tPLQZ			150	ns
Output Hold from F- $\overline{\text{CE}}$, $\overline{\text{OE}}$ and Address	tOH	tOH	0			ns
OE hold from $\overline{\text{WE}}$ High	tOEH	tWHGL	10			ns
F- $\overline{\text{RP}}$ Recovery to $\overline{\text{CE}}$ Low	tPS	tPHEL	150			ns

Notes : 1. Timing measurements are made under AC waveforms for read operation.

Read / Write Mode ($\overline{\text{WE}}$ Control)

Parameter	Symbol		Vcc=2.7V~3.3V			Unit
			Min	Typ	Max	
Write Cycle Time	tWC	tAVAV	85			ns
Address Setup Time	tAS	tAVWH	35			ns
Address Hold Time	tAH	tWHAX	0			ns
Data Setup time	tDS	tDVWH	35			ns
Data Hold time	tDH	tWHDX	0			ns
$\overline{\text{OE}}$ Hold from $\overline{\text{WE}}$ High	tOEH	tWHGL	10			ns
Chip Enable Setup Time	tCS	tELWL	0			ns
Chip Enable Hold Time	tCH	tWHEH	0			ns
Write Pulse Width	tWP	tWLWH	35			ns
Write Pulse Width High	tWPH	tWHWL	30			ns
$\overline{\text{OE}}$ Hold to $\overline{\text{WE}}$ Low	tGHWL	tGHWL	0			ns
Block Lock Setup to Write Enable High	tBLS	tPHHWH	85			ns
Block Lock Hold from Valid SRD	tBLH	tQVPH	0			ns
Duration of Auto Program Operation (Word Mode)	tDAP	tWHRH1		30	300	μs
Duration of Auto Program Operation (Page Mode)	tDAP	tWHRH1		4	80	ms
Duration of Auto Block Erase Operation	tDAE	tWHRH2		150	600	ms
Delay Time to Begin Internal Operation	tWHRL	tWHRL			85	ns
F- $\overline{\text{RP}}$ Recovery to F- $\overline{\text{CE}}$ Low	tPS	tPHWL	150			ns

Notes : 1. Read timing parameters during command write operations mode are the same as during read only operation mode.
2. Typical values at F-Vcc=3.0V and Ta=25°C.

AC CHARACTERISTICS

Read / Write Mode ($\overline{\text{CE}}$ Control)

Parameter	Symbol		Vcc=2.7V~3.3V			Unit
			Min	Typ	Max	
Write Cycle Time	tWC	tAVAV	85			ns
Address Setup Time	tAS	tAVWH	35			ns
Address Hold Time	tAH	tWHAX	0			ns
Data Setup Time	tDS	tDVWH	35			ns
Data Hold Time	tDH	tWHDX	0			ns
$\overline{\text{OE}}$ Hold from $\overline{\text{WE}}$ High	tOEH	tWHGL	10			ns
Write Enable Setup Time	tWS	tWLEL	0			ns
Write Enable Hold Time	tWH	tEWHH	0			ns
F- $\overline{\text{CE}}$ Pulse Width	tCEP	tELEH	35			ns
F- $\overline{\text{CE}}$ "H" Pulse Width	tCEPH	tEHEL	30			ns
$\overline{\text{OE}}$ Hold to $\overline{\text{WE}}$ Low	tGHEL	tGHEL	85			ns
Block Lock Setup to Write Enable High	tBLS	tPHHWH	85			ns
Block Lock Hold from Valid SRD	tBLH	tQVPH	0			ns
Duration of Auto Program Operation (Word Mode)	tDAP	tWHRH1		30	300	μs
Duration of Auto Program Operation (Page Mode)	tDAP	tWHRH1		4	80	ms
Duration of Auto Block Erase Operation	tDAE	tWHRH2		150	600	ms
Delay Time to Begin Internal Operation	tEHRL	tEHRL			90	ns
F- $\overline{\text{RP}}$ Recovery to F- $\overline{\text{CE}}$ Low	tPS	tPHWL	150			ns

- Notes : 1. Timing measurements are made under AC waveforms for read operations
2. Typical values at F-Vcc=3.0V and Ta=25°C.

Program / Erase Time

Parameter	Min	Typ	Max	Unit
Block Erase Time		150	600	ms
Main Block Write Time		1	4	sec
Page Write Time		4	80	ms
Flash to Page Buffer Time		100	150	μs

Program Suspend / Erase Suspend Time

Parameter	Min	Typ	Max	Unit
Program Suspend Time			15	μs
Erase Suspend Time			15	μs

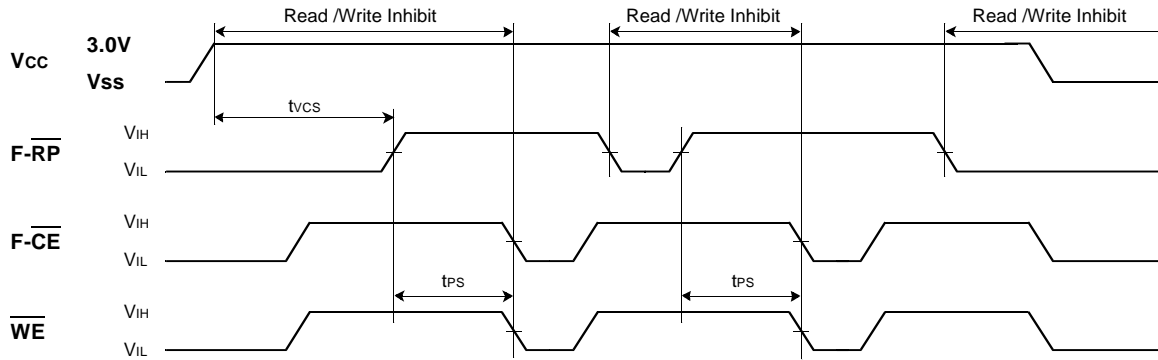
F-Vcc Power up / Down timing

Parameter	Min	Typ	Max	Unit
tVCS	F- $\overline{\text{RP}}=V_{IH}$ Setup Time from F-Vcc min.	2	15	μs

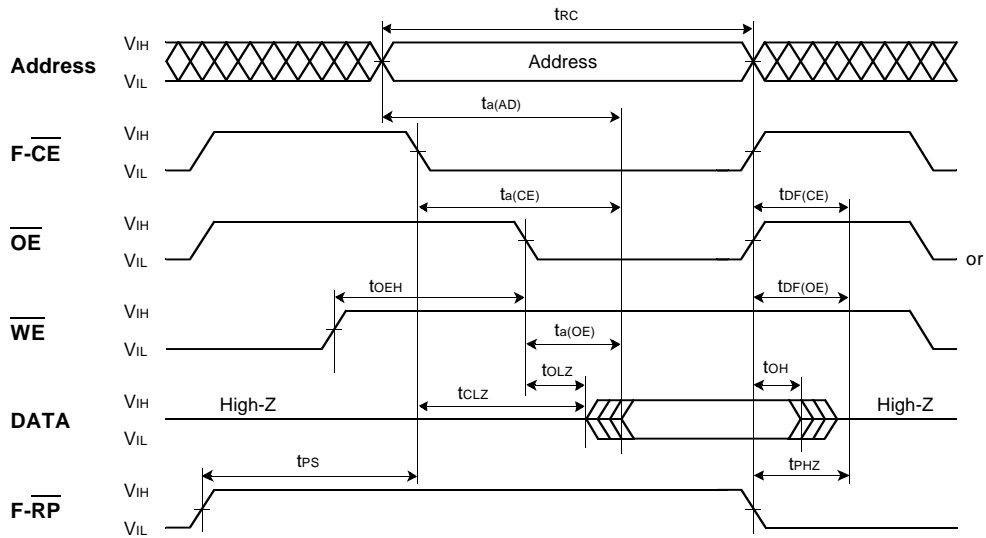
Please see 21 page.

During power up / down, by the noise pulses on control pins, the device has possibility of accidental erase of programming. The device must be protected against initiation of write cycle for memory contents during power up / down. The delay time of min. 2 micro sec is always required before read operation or write operation is initiated from the time F-Vcc reaches F-Vcc min. during power up /down. By holding F- $\overline{\text{RP}}=V_{IL}$, the contents of memory is protected during F-Vcc power up / down. During power up, F- $\overline{\text{RP}}$ must be held V_{IL} for min. 2us from the time F-Vcc reaches F-Vcc min.. During power down, F- $\overline{\text{RP}}$ must be held V_{IL} until F-Vcc reaches Vss. F- $\overline{\text{RP}}$ doesn't have latch mode, therefore F- $\overline{\text{RP}}$ must be held V_{IH} during read operation or erase / program operation.

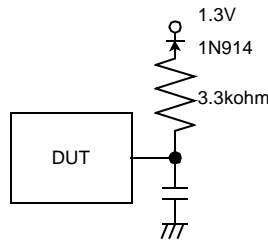
F-Vcc Power up / down Timing



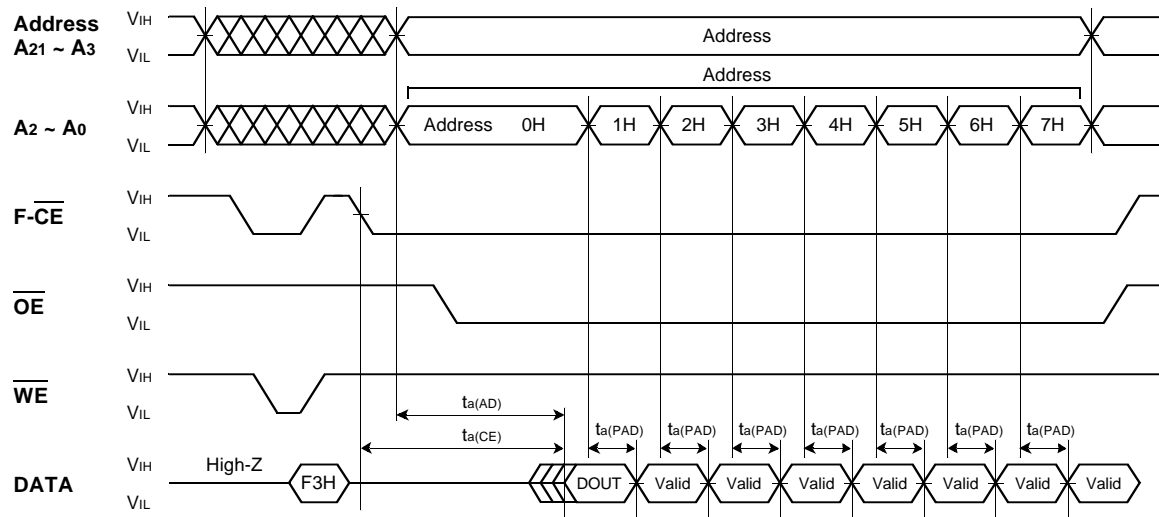
AC Waveforms for Read Operation and Test Conditions



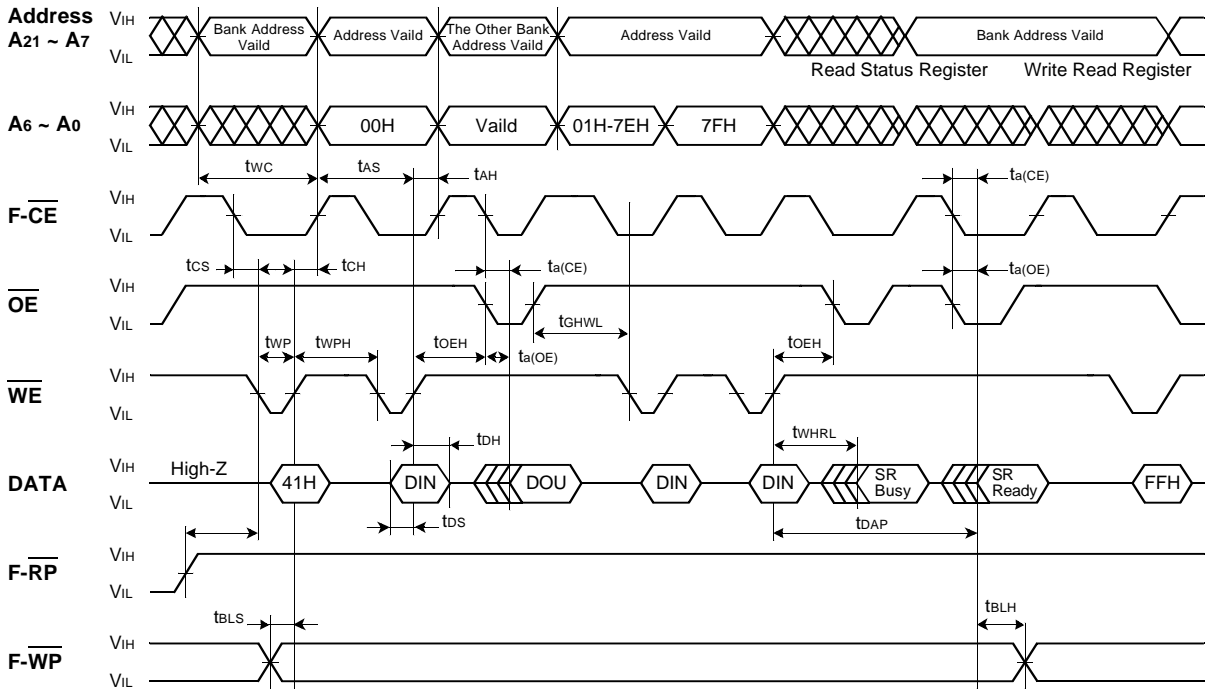
TEST CONDITIONS
 FOR AC CHARACTERISTICS
 Input Voltage: $V_{IL}=0V$, $V_{IH}=\text{Flash } V_{CC}$
 Input Rise and Fall Times: $\leq 5ns$
 Reference Voltage
 at timing measurement: $(\text{Flash } V_{CC})/2$
 Output Load: 1TTL gate + $CL(30pF)$



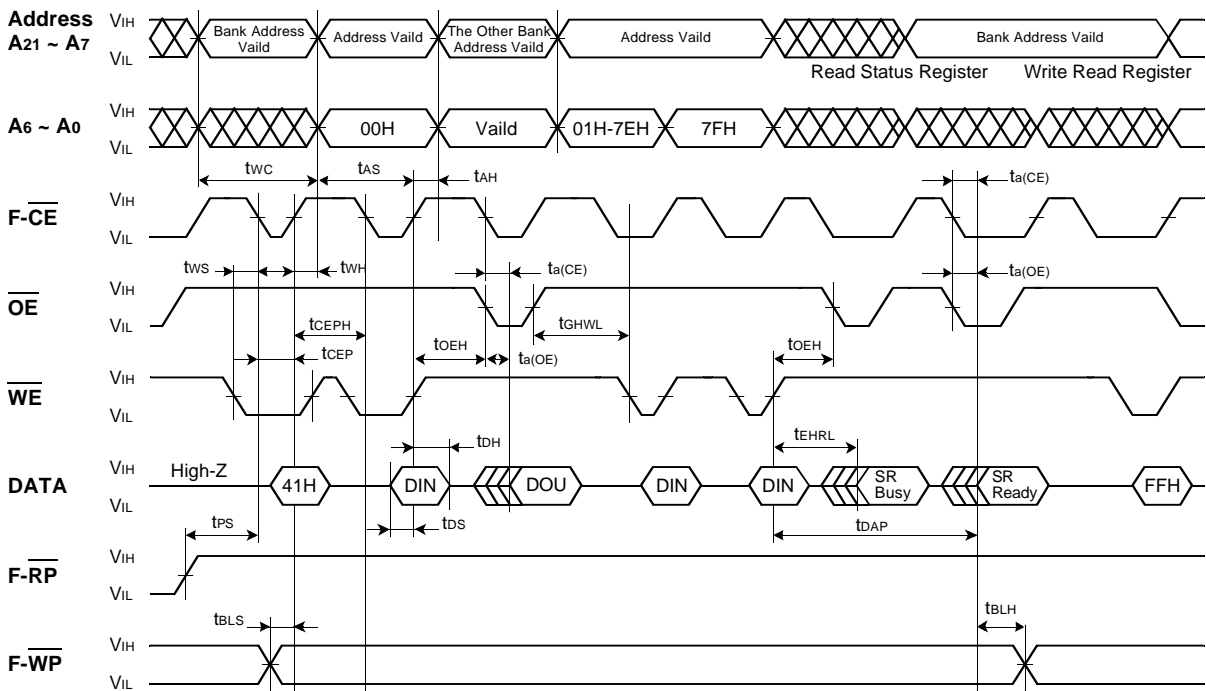
AC Waveforms for Sequential Page Read Operation



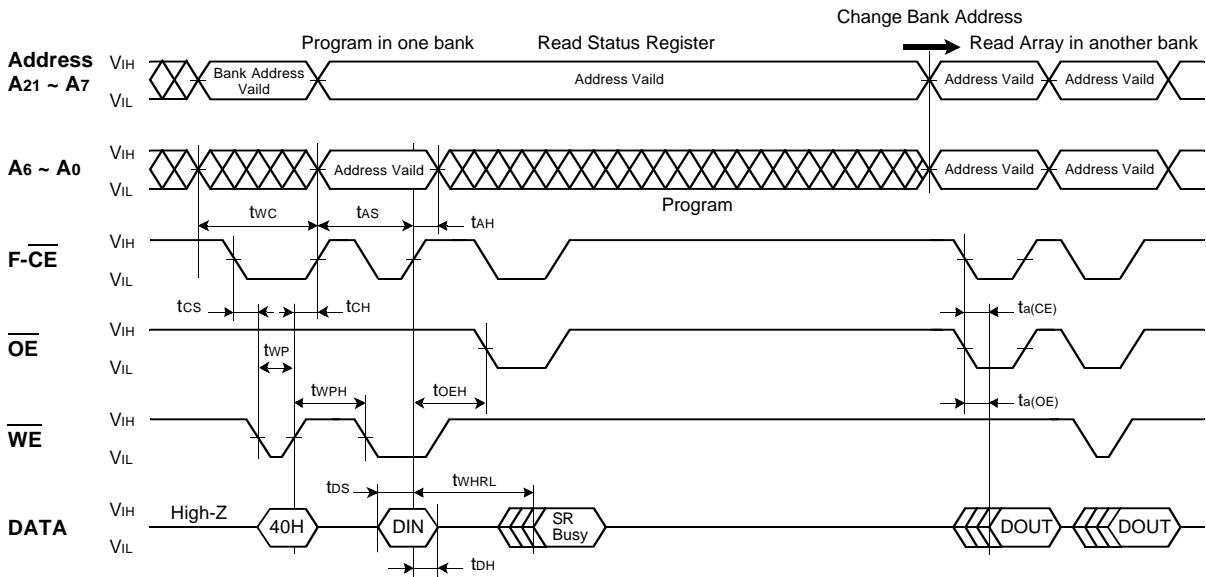
AC Waveforms for Page Program Operation(\overline{WE} Control)



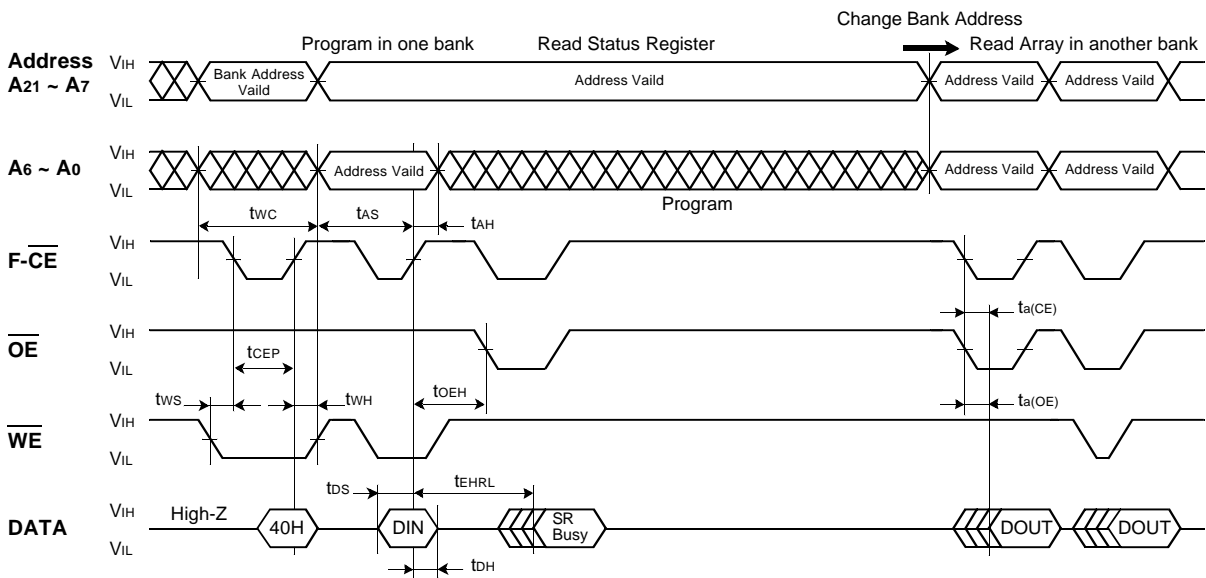
AC Waveforms for Page Program Operation(\overline{CE} Control)



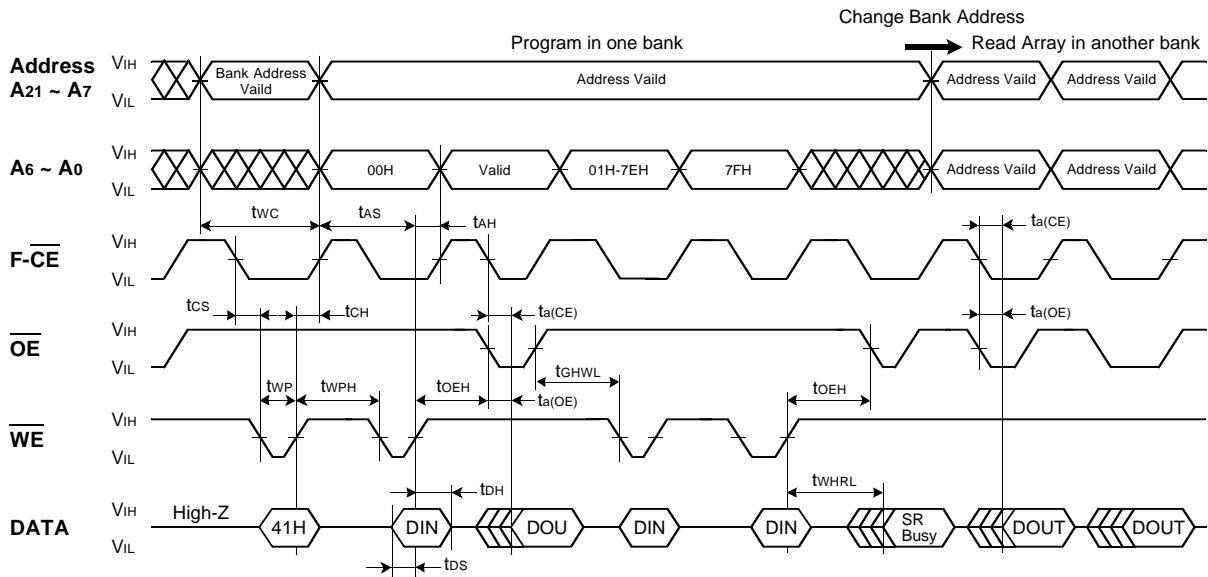
AC Waveforms for Word Program Operation with BGO(\overline{WE} Control)



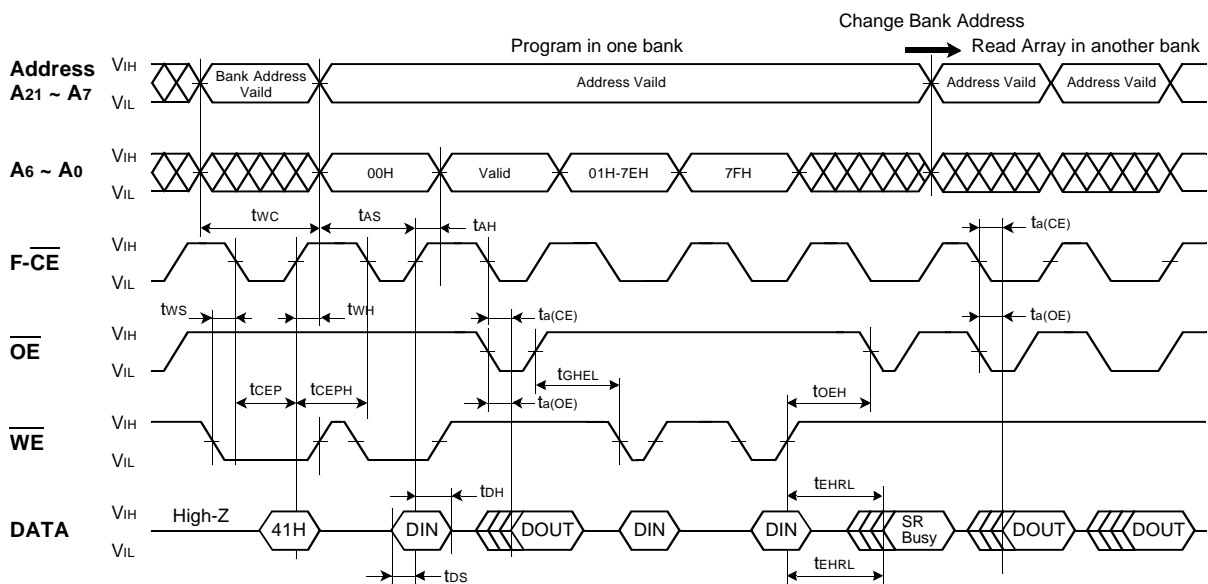
AC Waveforms for Word Program Operation with BGO(\overline{CE} Control)



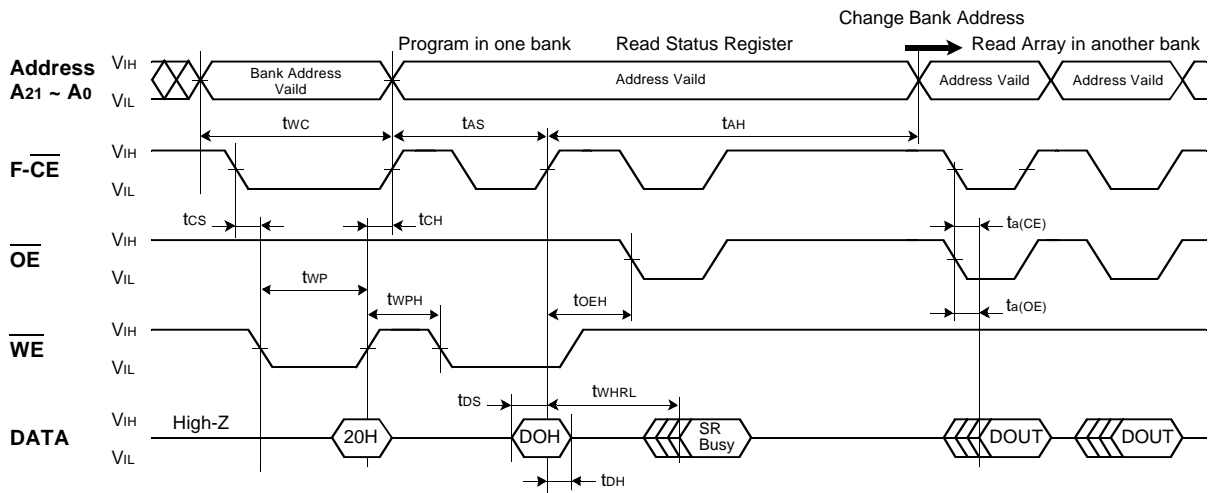
AC Waveforms for Page Program Operatio with BGO(\overline{WE} Control)



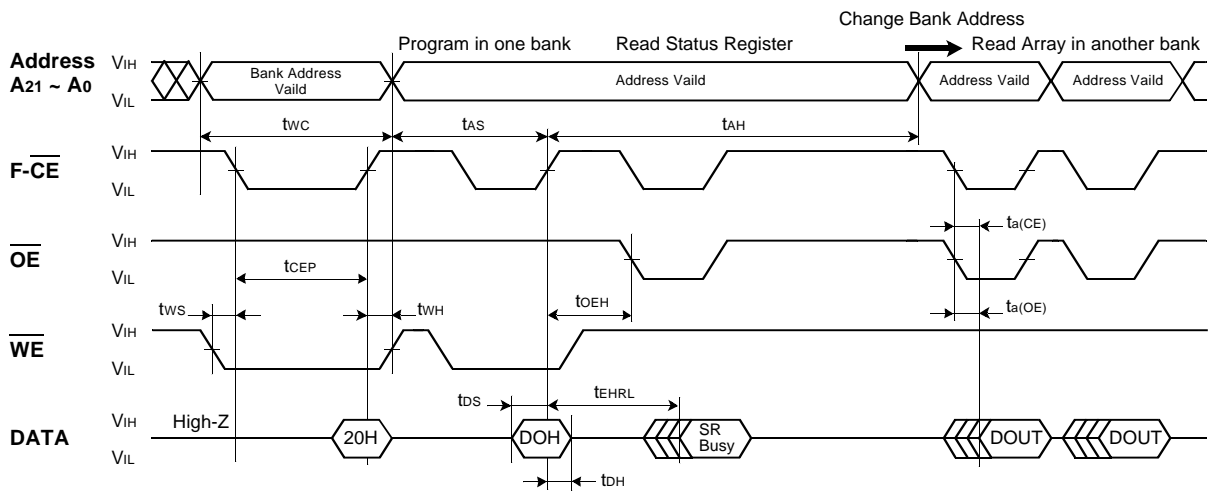
AC Waveforms for Page Program Operatio with BGO(\overline{CE} Control)



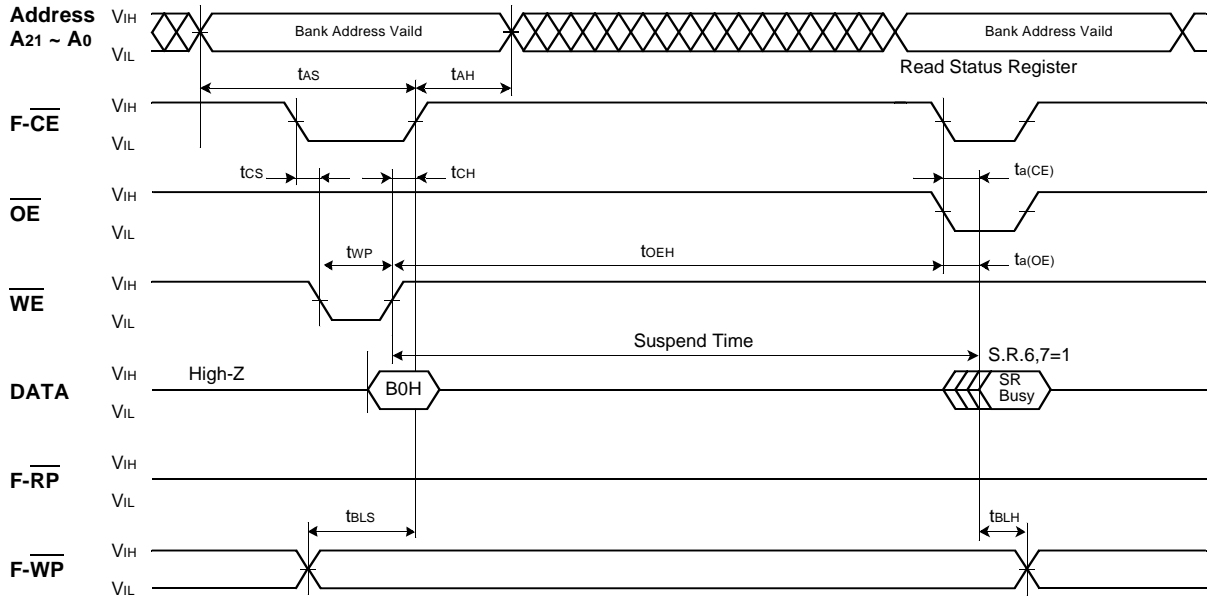
AC Waveforms for Erase Operation with BGO(\overline{WE} Control)



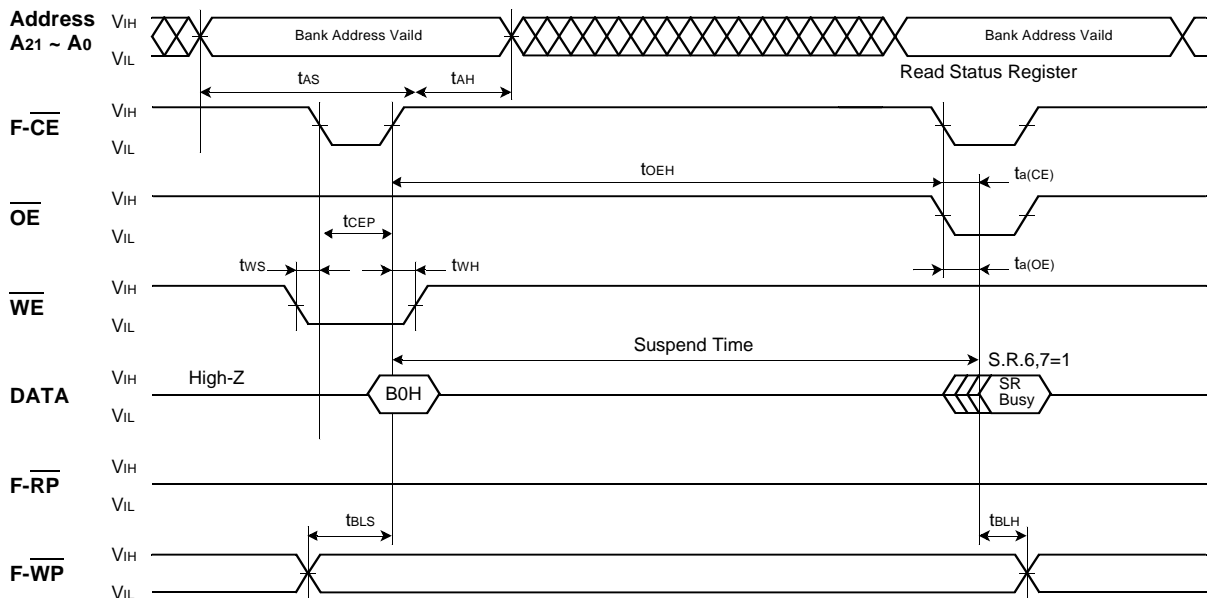
AC Waveforms for Erase Operation with BGO(\overline{CE} Control)



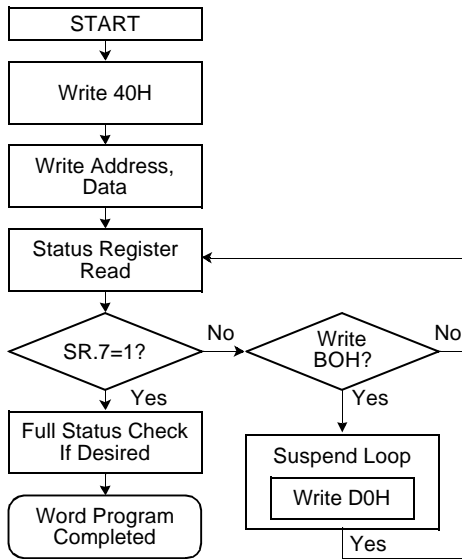
AC Waveforms for Suspend Operation($\overline{\text{WE}}$ Control)



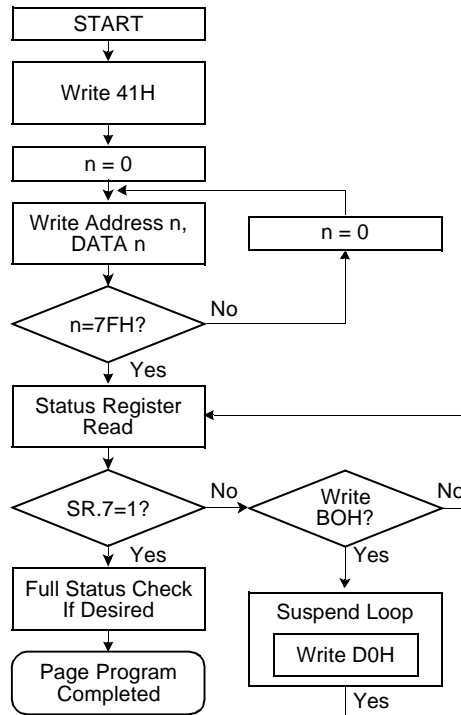
AC Waveforms for Suspend Operation($\overline{\text{CE}}$ Control)



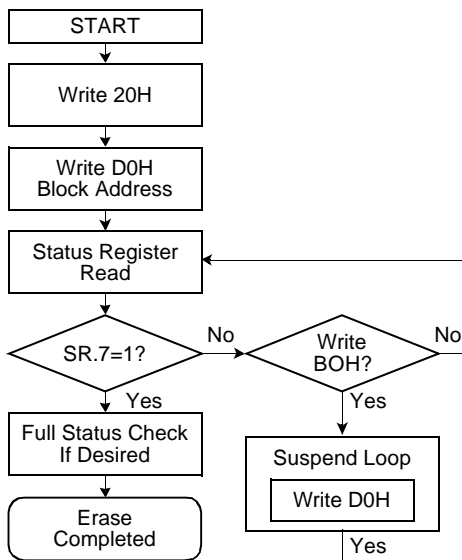
Word Program Flow Chart



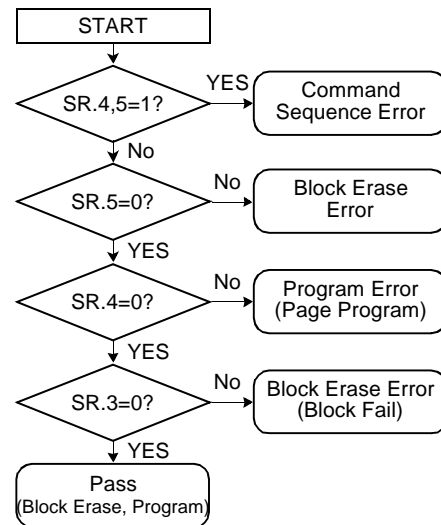
Page Program Flow Chart



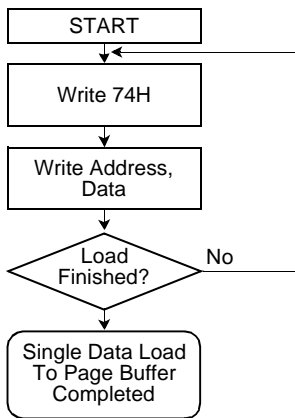
Block Erase Flow Chart



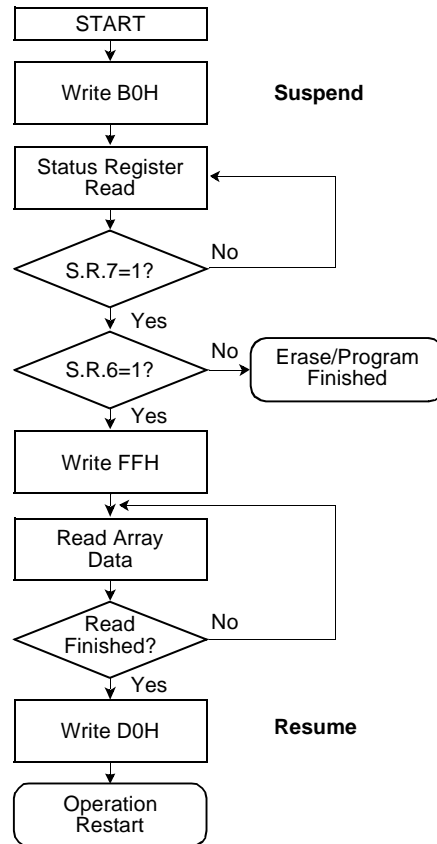
Status Register Check Flow Chart



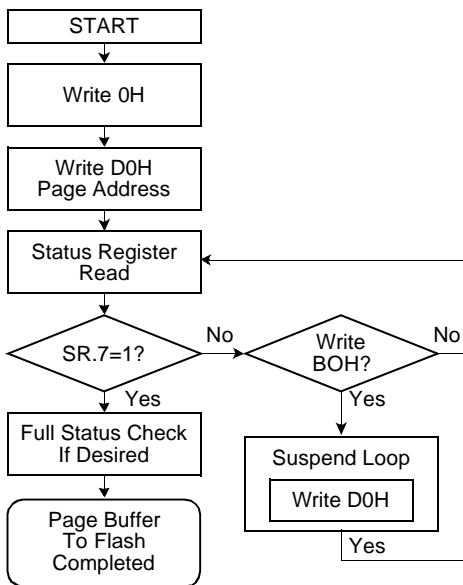
Single Data Load to Page Buffer Flow Chart



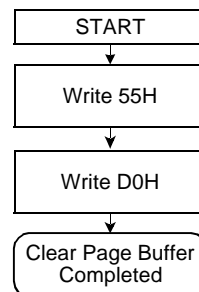
Suspend / Resume Flow Chart



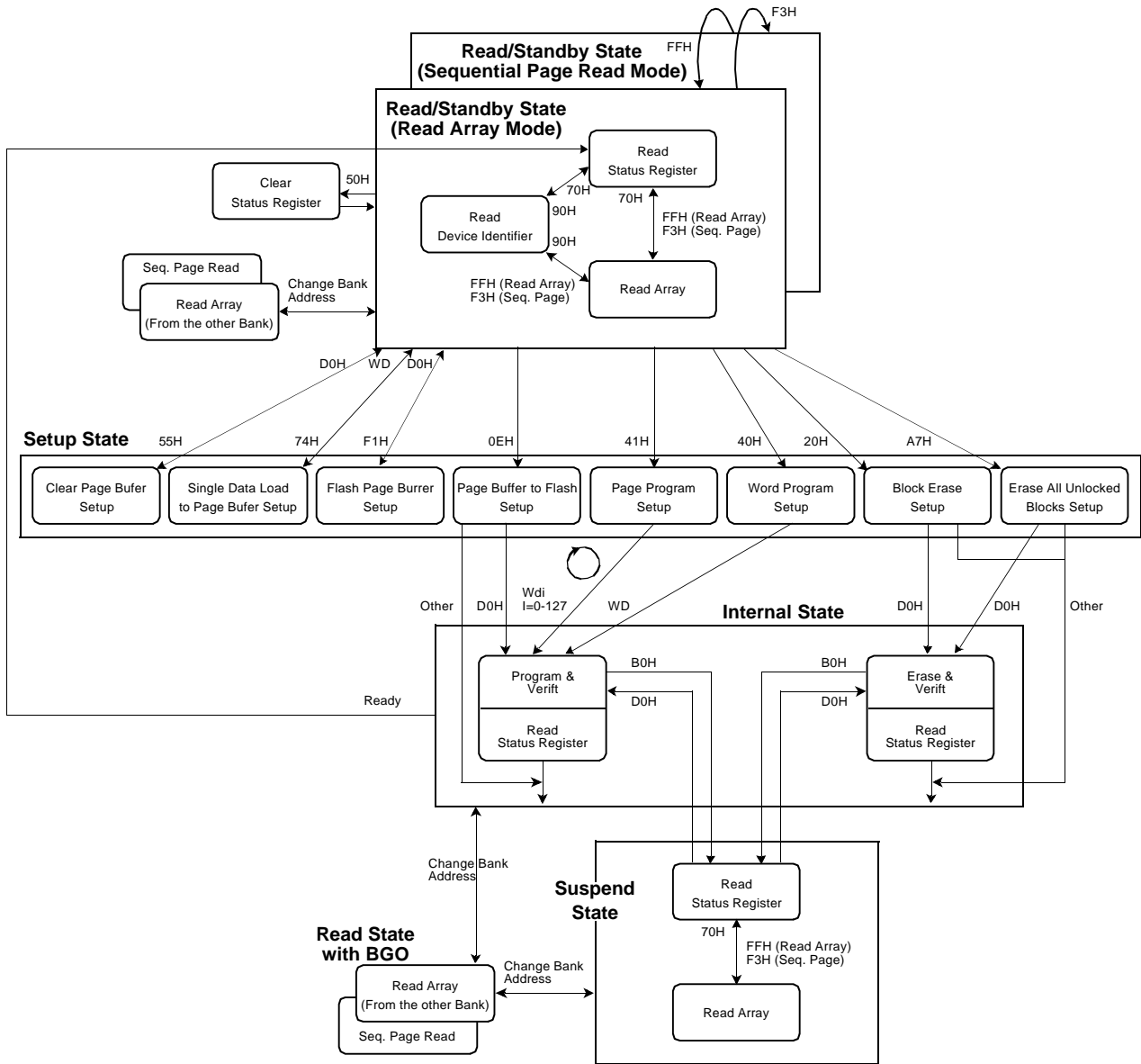
Page Buffer to Flash Flow Chart



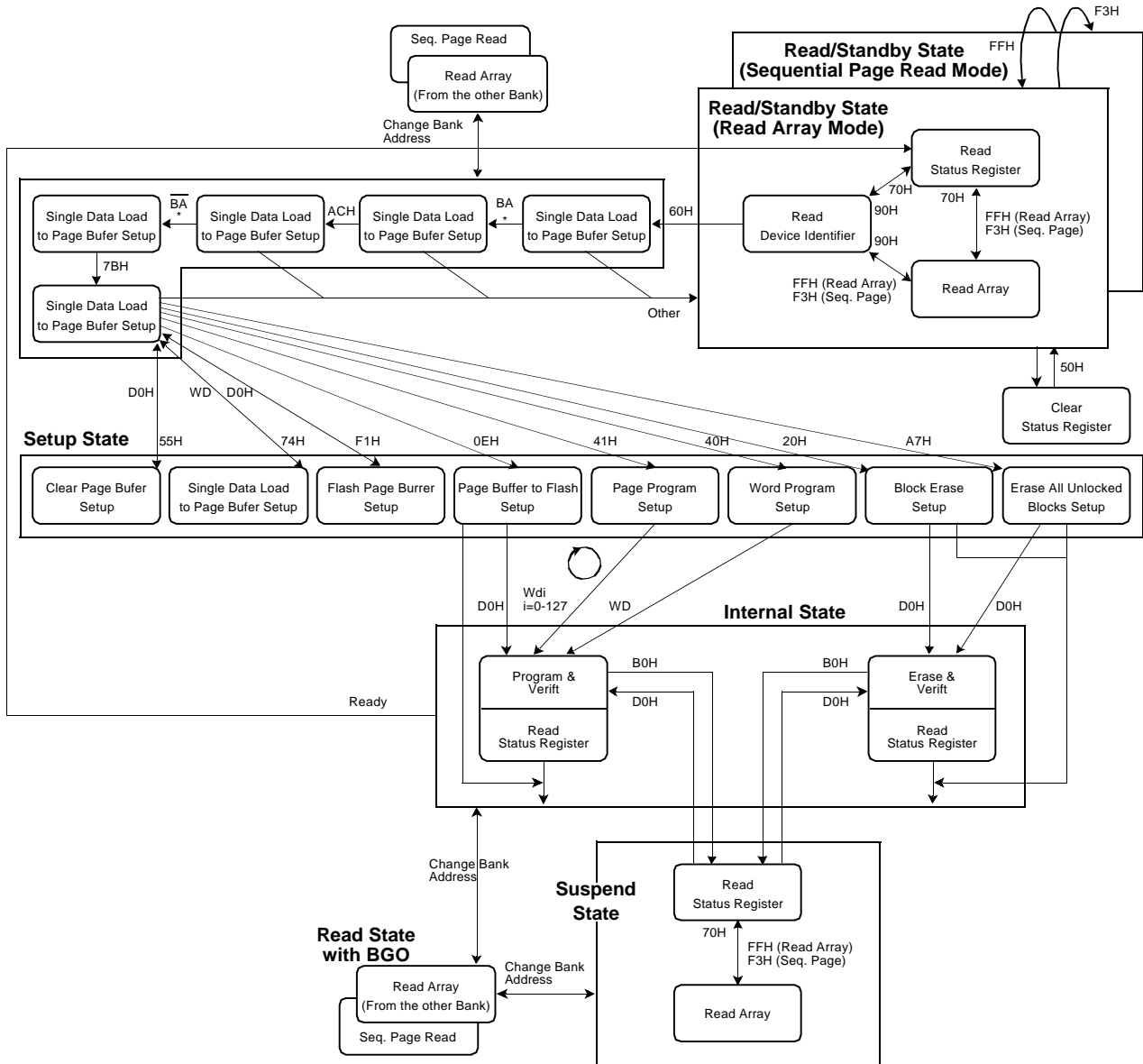
Clear Page Buffer Flow Chart



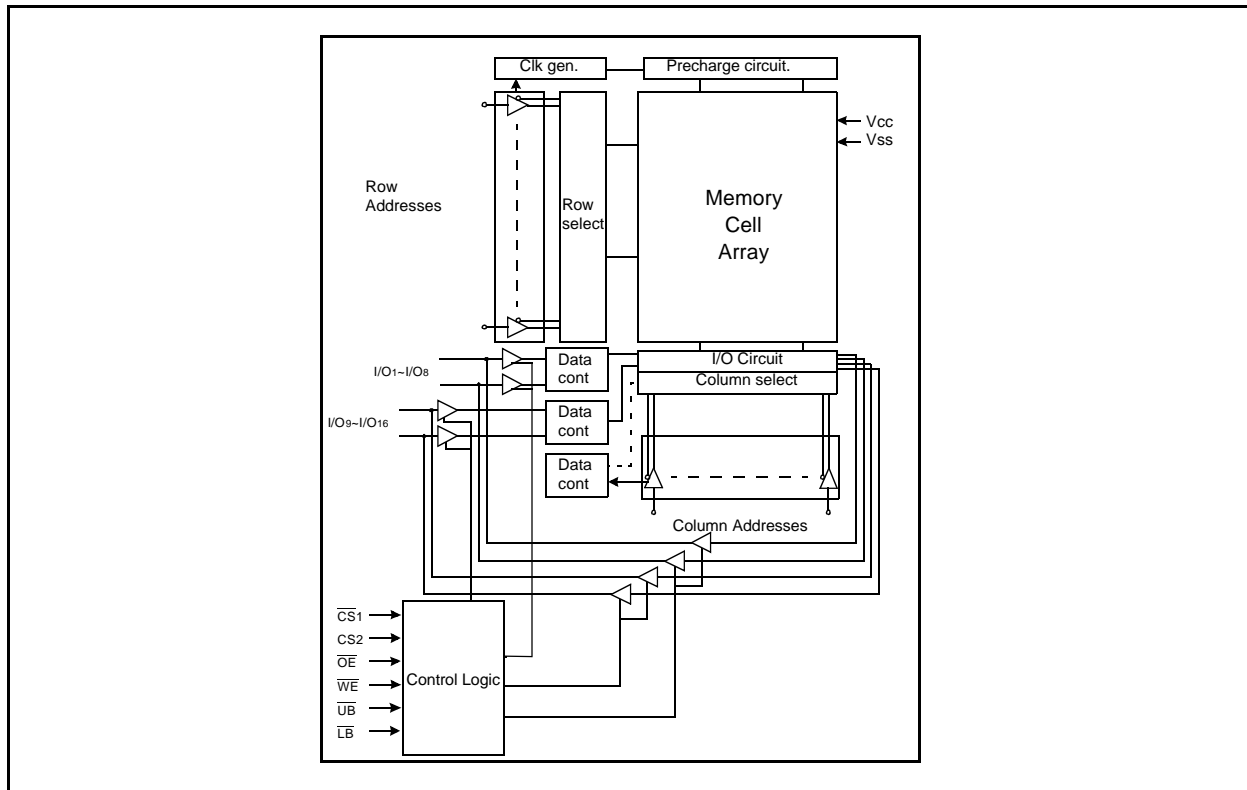
Operation Status ($\overline{WP}=VIH$)



Operation Status ($\overline{WP}=V_{IL}$)



SRAM Part



FUNCTIONAL BLOCK DIAGRAM (16Mbit SRAM)

FUNCTIONAL DESCRIPTION

$\overline{CS1}$	$CS2$	\overline{OE}	\overline{WE}	\overline{LB}	\overline{UB}	I/O1-8	I/O9-16	Mode	Power
H	X ⁽¹⁾	X ⁽¹⁾	X ⁽¹⁾	X ⁽¹⁾	X ⁽¹⁾	High-Z	High-Z	Deselected	Standby
X ⁽¹⁾	L	X ⁽¹⁾	X ⁽¹⁾	X ⁽¹⁾	X ⁽¹⁾	High-Z	High-Z	Deselected	Standby
X ⁽¹⁾	X ⁽¹⁾	X ⁽¹⁾	X ⁽¹⁾	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X ⁽¹⁾	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X ⁽¹⁾	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	Word Read	Active
L	H	X ⁽¹⁾	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	X ⁽¹⁾	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	X ⁽¹⁾	L	L	L	Din	Din	Word Write	Active

1. X means don't care. (Must be low or high state)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.2 to V _{CC} +0.3V(Max. 3.6V)	V
Voltage on Vcc supply relative to Vss	V _{CC}	-0.2 to 3.6	V
Power Dissipation	P _D	1.0	W
Storage temperature	T _{STG}	-65 to 150	°C
Operating Temperature	T _A	-40 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	2.7	3.0	3.3	V
Ground	V _{SS}	0	0	0	V
Input high voltage	V _{IH}	2.2	-	V _{CC} +0.2 ²⁾	V
Input low voltage	V _{IL}	-0.2 ³⁾	-	0.6	V

Note:

1. T_A=-40 to 85°C, otherwise specified
2. Overshoot: V_{CC}+2.0V in case of pulse width ≤20ns.
3. Undershoot: -2.0V in case of pulse width ≤20ns.
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ ¹⁾	Max	Unit
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA
Output leakage current	I _{LO}	$\overline{CS}1=V_{IH}$ or $CS2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ or $\overline{LB}=\overline{UB}=V_{IH}$, V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA
Average operating current	I _{CC1}	Cycle time=1μs, 100%duty, I _{IO} =0mA, $\overline{CS}1\leq 0.2V$, $\overline{LB}\leq 0.2V$ or/and $\overline{UB}\leq 0.2V$, $CS2\geq V_{CC}-0.2V$, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	-	-	4	mA
	I _{CC2}	Cycle time=Min, I _{IO} =0mA, 100% duty, $\overline{CS}1=V_{IL}$, $CS2=V_{IH}$, $\overline{LB}=V_{IL}$ or/and $\overline{UB}=V_{IL}$, V _{IN} =V _{IL} or V _{IH}	55ns	-	30	35
Output low voltage	V _{OL}	I _{OL} = 2.1mA	-	-	0.4	V
Output high voltage	V _{OH}	I _{OH} = -1.0mA	2.4	-	-	V
Standby Current (CMOS)	I _{SB1}	Other input =0~V _{CC} 1) $\overline{CS}1\geq V_{CC}-0.2V$, $CS2\geq V_{CC}-0.2V$ ($\overline{CS}1$ controlled) or 2) $0V\leq CS2\leq 0.2V$ ($CS2$ controlled) or 3) $\overline{LB}=\overline{UB}\geq V_{CC}-0.2V$, $CS2\geq V_{CC}-0.2V$ ($\overline{LB}/\overline{UB}$ controlled)	-	0.5	20	μA

1. Typical value are measured at V_{CC}=3.0V, T_A=25°C and not 100% tested.

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Input/Output Reference)

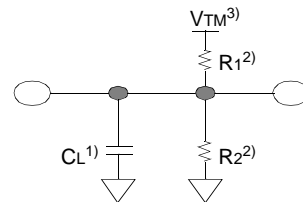
Input pulse level: 0.4 to 2.2V

Input rising and falling time: 5ns

Input and output reference voltage: 1.5V

Output load (see right): $C_L = 100\text{pF} + 1\text{TTL}$

$C_L = 30\text{pF} + 1\text{TTL}$



1. Including scope and jig capacitance
2. $R_1 = 3070\Omega$, $R_2 = 3150\Omega$
3. $V_{TM} = 2.8\text{V}$

AC CHARACTERISTICS

Parameter List		Symbol	55ns		Units
			Min	Max	
Read	Read cycle time	tRC	55	-	ns
	Address access time	tAA	-	55	ns
	Chip select to output	tCO1, tCO2	-	55	ns
	Output enable to valid output	tOE	-	30	ns
	\overline{UB} , \overline{LB} Access Time	tBA	-	55	ns
	Chip select to low-Z output	tLZ1, tLZ2	10	-	ns
	\overline{UB} , \overline{LB} enable to low-Z output	tBLZ	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	ns
	Chip disable to high-Z output	tHZ1, tHZ2	0	20	ns
	\overline{UB} , \overline{LB} disable to high-Z output	tBHZ	0	20	ns
	Output disable to high-Z output	tOHZ	0	20	ns
Output hold from address change	tOH	10	-	ns	
Write	Write cycle time	tWC	55	-	ns
	Chip select to end of write	tCW	45	-	ns
	Address set-up time	tAS	0	-	ns
	Address valid to end of write	tAW	45	-	ns
	\overline{UB} , \overline{LB} Valid to End of Write	tBW	45	-	ns
	Write pulse width	tWP	40	-	ns
	Write recovery time	tWR	0	-	ns
	Write to output high-Z	tWHZ	0	20	ns
	Data to write time overlap	tDW	20	-	ns
	Data hold from write time	tDH	0	-	ns
	End write to output low-Z	tOW	5	-	ns

SRAM DATA RETENTION CHARACTERISTICS

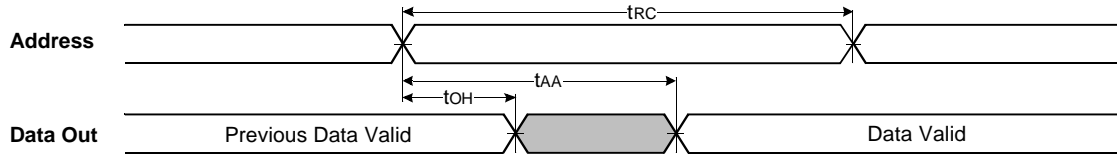
Item	Symbol	Test Condition	Min	Typ	Max	Unit
Vcc for data retention	VDR	$\overline{CS1} \geq V_{cc} - 0.2\text{V}$	1.5	-	3.3	V
Data retention current	IDR	$V_{cc} = 3.0\text{V}$, $\overline{CS1} \geq V_{cc} - 0.2\text{V}$	-	0.5	20	μA
Data retention set-up time	tSDR	See data retention waveform	0	-	-	ns
Recovery time	tRDR		tRC	-	-	

1. $\overline{CS1} \geq V_{cc} - 0.2\text{V}$, $\overline{CS2} \geq V_{cc} - 0.2\text{V}$ ($\overline{CS1}$ controlled) or $\overline{CS2} \leq 0.2\text{V}$ ($\overline{CS2}$ controlled)

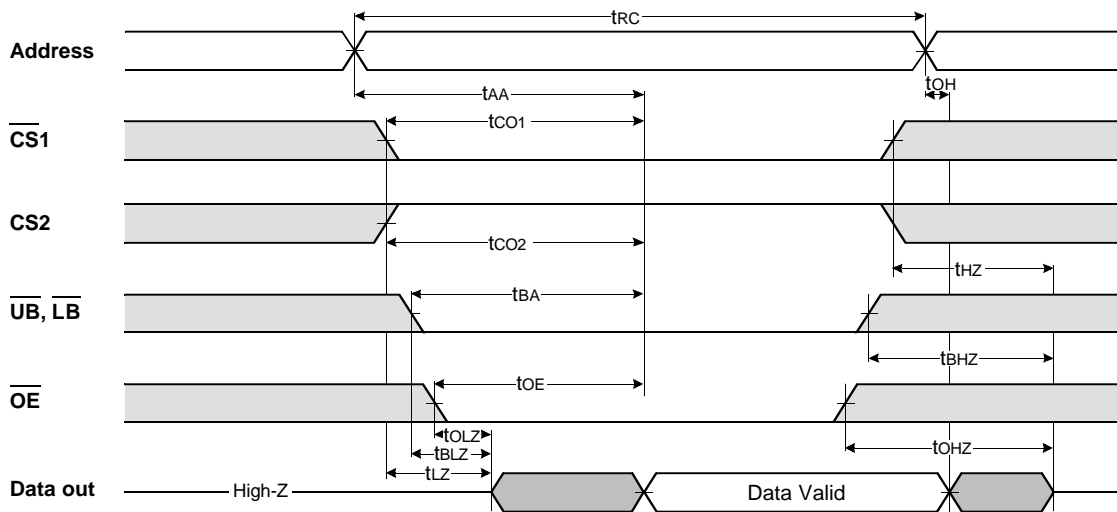
2. Typical values are measured at $V_{cc} = 3.0\text{V}$, $T_a = 25^\circ\text{C}$, not 100% tested.

SRAM TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS1}=\overline{OE}=V_{IL}$, $CS2=\overline{WE}=V_{IH}$, \overline{UB} or/and $\overline{LB}=V_{IL}$)



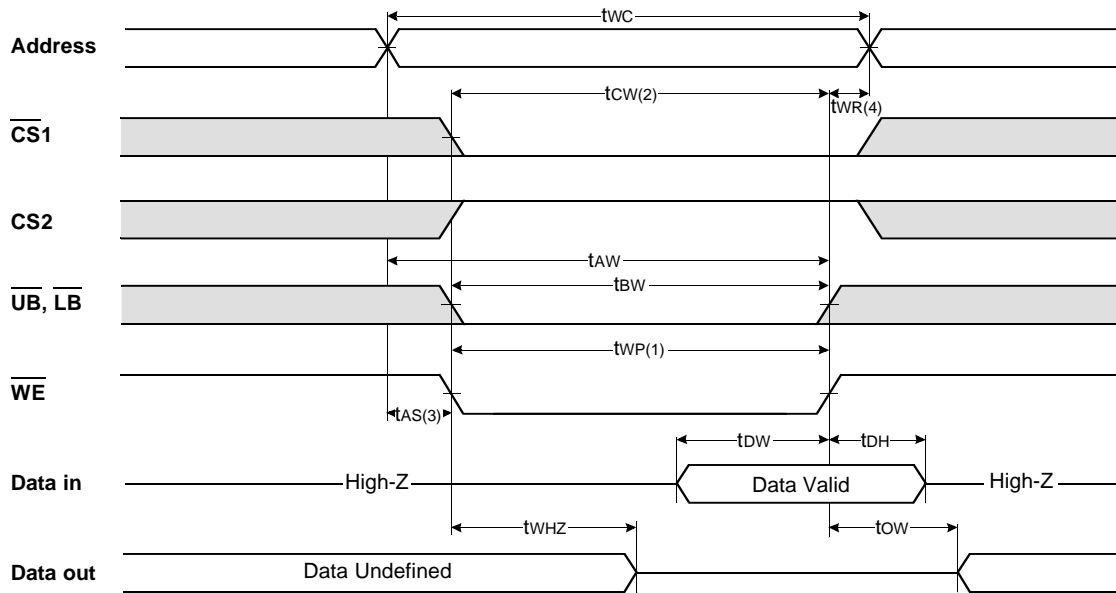
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



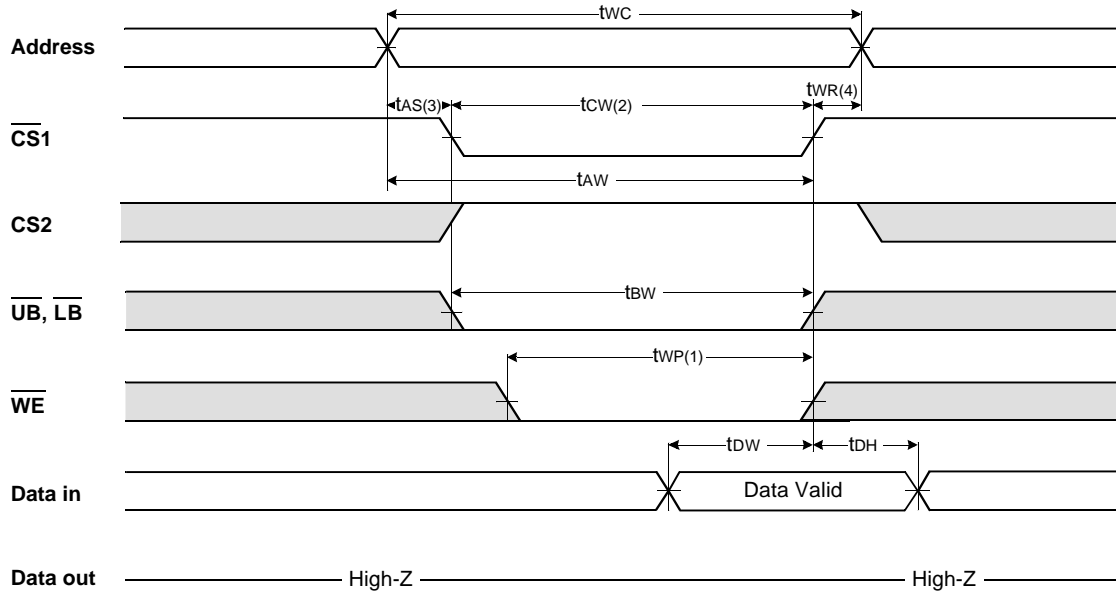
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

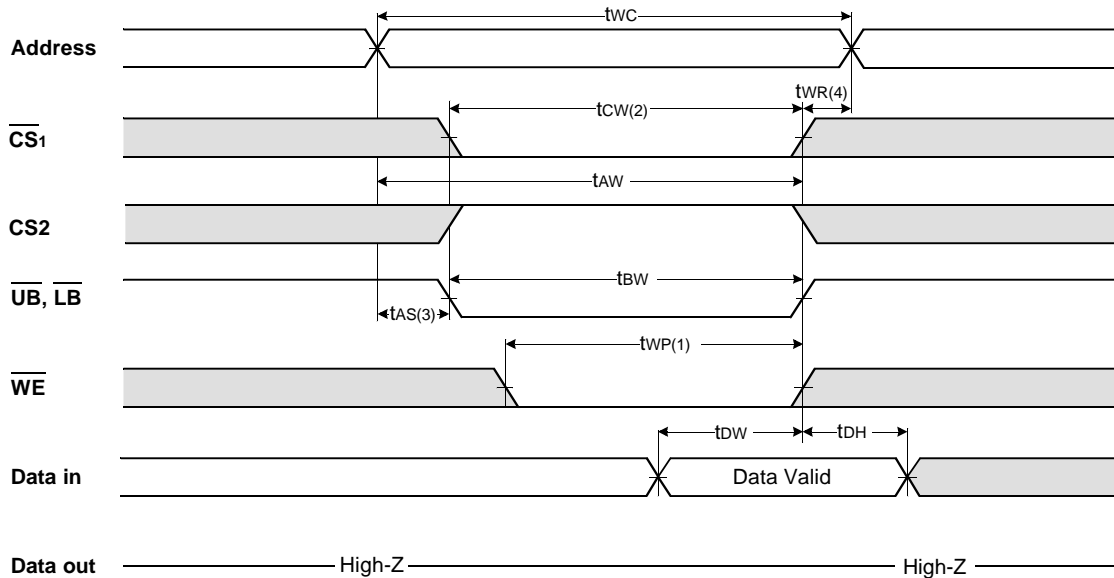
TIMING WAVEFORM OF WRITE CYCLE(1) (\overline{WE} Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (\overline{UB} , \overline{LB} Controlled)

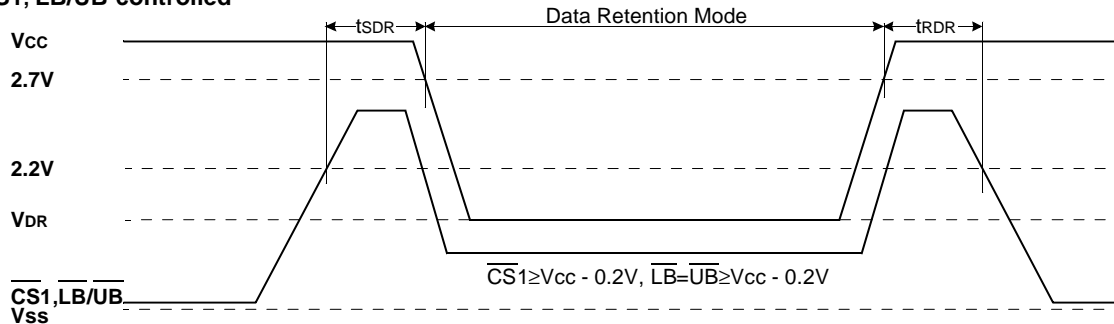


NOTES (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of low $\overline{CS1}$ and low \overline{WE} . A write begins when $\overline{CS1}$ goes low and \overline{WE} goes low with asserting \overline{UB} or \overline{LB} for single byte operation or simultaneously asserting \overline{UB} and \overline{LB} for double byte operation. A write ends at the earliest transition when $\overline{CS1}$ goes high and \overline{WE} goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS1}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS1}$ or \overline{WE} going high.

DATA RETENTION WAVE FORM

$\overline{CS1}$, $\overline{LB}/\overline{UB}$ controlled



CS2 controlled

